

FT61F02X

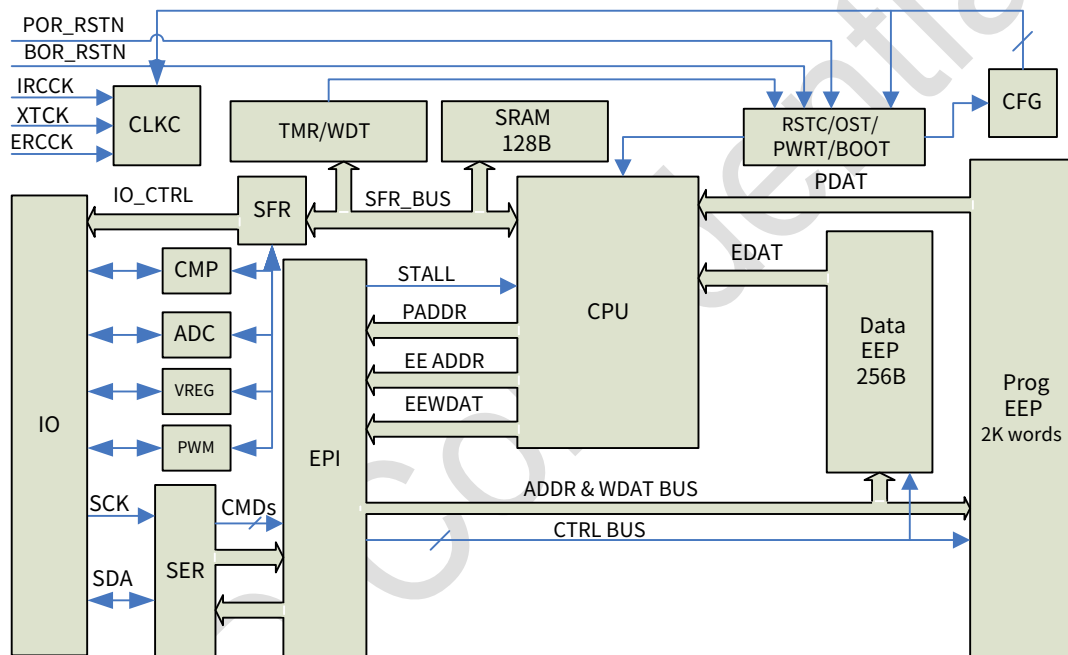
DATA SHEET

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1characteristic

- Independent Intellectual Property Reduced Instruction Set
- 8layer hardware stackx11bit
- 2T or 4T instruction cycle
- 2Kx14b program memory
 - program memory space checksum automatic calibration
 - Configurable, User Option
- 256x8b data EEPROM
 - data EEPROM In-App Programming High
- Endurance EEPROM
 - program and data EEPROM can withstand 100 million write
 - operations EEPROM save time > 40 year
- 128x8b SRAM
- 1x bring 8bit prescaled timer0 1x
- bring 3bit prescaler 16bit timer1 1x
- bring 8bit prescaled timer2
- Enhanced Capture, Compare and Programmable-dead zone || TimePWM module
 - Clock source optional: system clock or internal 32MHz Clock
 - One-Shot Mode
 - most 3 pair of belts-dead zone || of PWM output
- 3x 12bit Timer, 3x 12bit PWM, support BUZZER pattern band 7bit
- prescaler WDT, with an overflow frequency of about 16ms~2048ms
- Power-up delay counter PWRT
- low power mode SLEEP
- multiple wake-up sources, INT, port change interrupt, WDT and data EEPROM write complete, etc. built-in
- high-speed 16M RC oscillator
- built-in low speed 32K RC oscillator
- Support external crystal oscillator 16M or 32K, and the external clock mode
 - missing clock detection
 - Two-speed start mode
- built-in 10bit ADC, support 8 channels (7 external channels + 1 internal 1/4 VDD aisle)
 - Reference voltage optional: external Vref, VDD, internal 2V/3V built-in 2 high
- speed high precision comparator
 - Programmable Reference Voltage
 - Comparison results can be output directly
- low voltage reset LVR: 2.0V/2.2V/2.8V low voltage detection LVD
- :2.0V/2.4V/2.8V/3.0V/3.6V/4.2V Two regulated outputs:
-
- Each channel can output up to 32 Maximum
- voltage 14 general IO, 16 root chip pin

- 14 individual I/O with independent pull-up control
- 4 individual I/O with independent pull-down control
- port change interrupt, RA0~RA7
- Supports in-system programming ICSP
- Support online debugging, 3 hardware breakpoint
- program space protection
- Working voltage range: 2.0V~5.5V
- Operating temperature: -40~85°C
- Maximum Clock Operating Frequency: 16MHz
 - $f_{\text{SYS}}=8\text{MHz}$: 2.0V~2.7V f_{SYS}
 - $=16\text{MHz}$: 2.7V~5.5V
- Package type: SOP14, SOP16

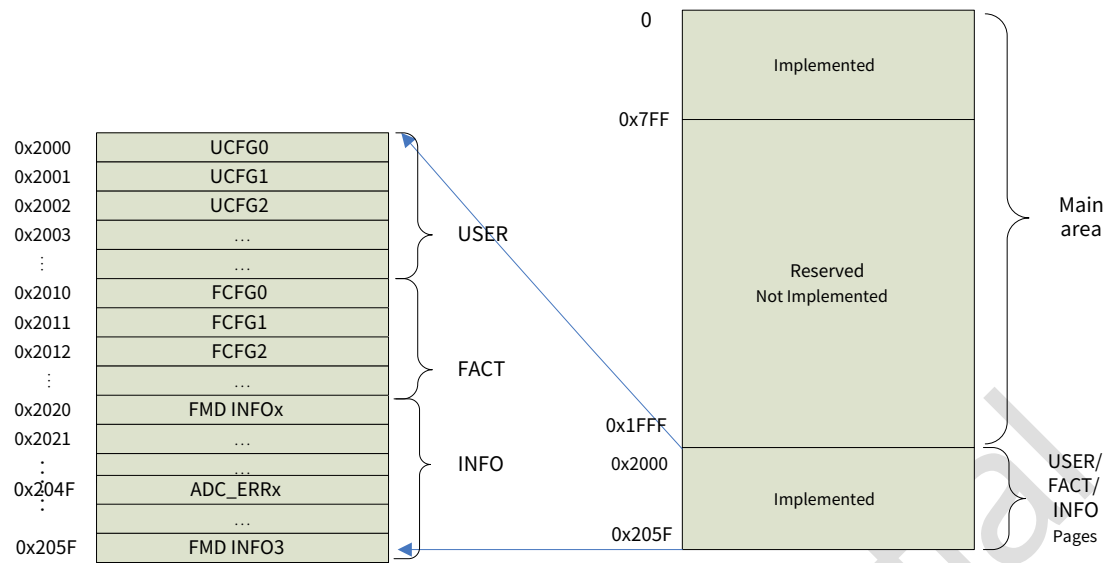


picture1.1 System functional block diagram

1.1 program memory

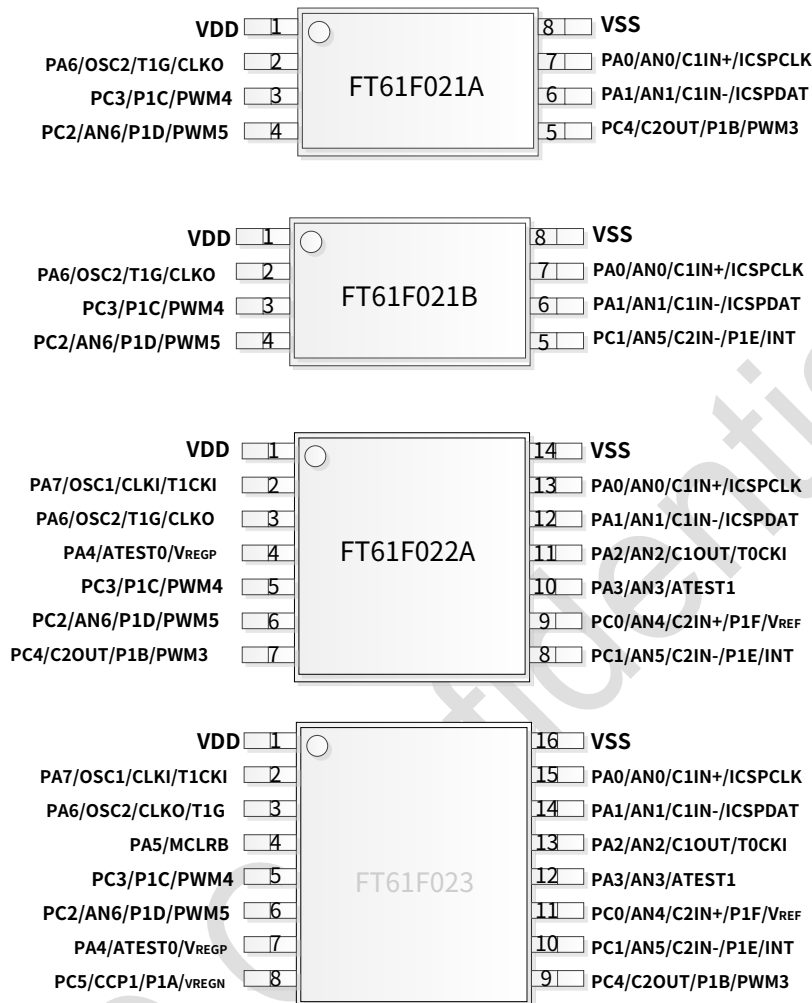
The address register is 13 bits (0x0000 ~ 0x1FFF), supporting up to 8K address space. The program memory has a total of 2K words (0x0000 ~ 0x07FF), plus 64 additional user configuration, factory configuration area, a total of 2K+64 words, they consist of EEPROM constitute. One PAGE is 16 words, the whole PROM is a total of 134 individual PAGE.

in 0~0x07FF Access to the main program area, the unimplemented part 0x800~0x1FFF reserve. user and factory configuration information area from 0x2000 start to 0x205F finish.



picture1.2Program Space Address Mapping

1.2 Footprint



picture1.3.1 FT61F02xPlanned footprint:SOP8,SOP14,SOP16

The following is a detailed description of the chip pins:

Pin name	function name	input letter number type	output letter number type	specific description	up and down
PA0/AN0/C1IN+/ICSPCLK	PA0	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up
	AN0	AN	—	A/Daisle0enter	
	ICSPCLK	ST	—	Debug/Burn mode string mouthclockSignal (Fmax=6MHz)	
	C1IN+	AN	—	Comparator1 non-inverting input	
PA1/AN1/C1IN-/ICSPDAT	PA1	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up
	AN1	AN	—	A/Daisle1enter	
	C1IN-	AN	—	Comparator1 inverting input	
	ICSPDAT	TTL	CMOS	Debug/Burn mode string mouthdataSignal (Fmax=6MHz)	
PA2/AN2/C1OUT/T0CKI	PA2	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up
	AN2	AN	—	A/Daisle2enter	
	C1OUT	—	CMOS	Comparator1 output	
	T0CKI	TTL	—	Timer 0source clock output enter (Fmax=4MHz)	
PA3/AN3/ATEST1	PA3	TTL	—	GPIO with IOC and WPU	Configurable pull-up
	AN3	AN	—	A/Daisle3enter	
	ATEST1	AN	AN	Analog Test Pins1	for internal testing
PA4/ATEST0/VREGP	PA4	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up/pull-down
	ATEST0	AN	AN	Analog Test Pins	for internal testing
	VREGP	—	AN	High voltage regulated output	
PA5/MCLRB	PA5	TTL	CMOS	GPIO with IOC and WPU(or input only)	Configurable pull-up
	MCLRB	TTL	—	External reset input	MCLRB
PA6/OSC2/T1G/CLKO	PA6	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up
	OSC2	—	XTAL	Crystal/Resonator	OSC2
	T1G	ST	—	Timer1Gating input	

	CLKO	—	CMOS	Test clock output (Fmax=10MHz)	CLKO
PA7/OSC1/CLKI/T1CKI	PA7	TTL	CMOS	GPIO with IOC and WPU	Configurable pull-up
	CLKI	ST	—	external clock input/RC oscillator connection	
	OSC1	XTAL	—	Crystal/Resonator	
	T1CKI	ST	—	Timer1 external clock	
PC0/AN4/C2IN+/P1F/VREF	PC0	TTL	CMOS	PORTC I/O	Configurable pull-up
	AN4	AN	—	A/Daisle4 enter	
	C2IN+	AN	—	Comparator2 non-inverting input	
	P1F	—	CMOS	Enhanced PWM output	
	VREF	AN	—	A/D external reference voltage enter	
PC1/AN5/C2IN-/P1E/INT	PC1	TTL	CMOS	PORTC I/O	Configurable pull-up/ drop down
	AN5	AN	—	A/Daisle5 enter	
	C1IN-	AN	—	Comparator2 inverting input	
	P1E	—	CMOS	Enhanced PWM output	
	INT	TTL	—	External interrupt input	
PC2/AN6/P1D/PWM5	PC2	TTL	CMOS	PORTC I/O	Configurable pull-up/ drop down
	AN6	AN	—	A/Daisle6 enter	
	P1D	—	CMOS	Enhanced PWM output	
	PWM5	—	CMOS	PWM5 output	
PC3/P1C/PWM4	PC3	TTL	CMOS	PORTC I/O	Configurable pull-up/ drop down
	P1C	—	CMOS	Enhanced PWM output	
	PWM4	—	CMOS	PWM4 output	
PC4/C2OUT/P1B/PWM3	PC4	TTL	CMOS	PORTC I/O	Configurable pull-up
	C2OUT	—	CMOS	Comparator2 output	
	P1B	—	CMOS	Enhanced PWM output	
	PWM3	—	CMOS	PWM3 output	
PC5/CCP1/P1A/VREGN	PC5	TTL	CMOS	PORTC I/O	Configurable pull-up
	CCP1	ST	CMOS	capture input/compare output	
	P1A	—	CMOS	Enhanced PWM output	
	VREGN	—	AN	Low voltage regulated output	

Notice:

1. IOC: Interrupt on change, generic I/O
2. WPU: Weak pullup
3. ST: bring CMOS level Schmitt trigger input
4. AN: Analog input or output

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