

Innovating Energy Technology

http://www.fujielectric.com/products/semiconductor/ **FUJI POWER MOSFET**

Super J MOS[®] S1 series

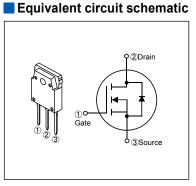
N-Channel enhancement mode power MOSFET

Features

Pb-free lead terminal **RoHS** compliant

Applications For switching

Outline Drawings [mm] TO-3P (+ + +)



Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	VDS	600	V	
Dialit-Source voltage	VDSX	600	V	V _{GS} =-30V
Continuous Drain Current	lo Rate	DD #41	А	Tc=25°C Note*1
		1102 #297 月日	А	Tc=100°C Note*1
Pulsed Drain Current	IDP/	A BS±14PLAP	A	Note*1
Gate-Source Voltage	VGs C D	5 × ±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	MAR 2	diffet	A	Note *2
Non-Repetitive Maximum Avalanche Energy	Ence IPI	1689.9 F	す∘ mJ	Note *3
Maximum Drain-Source dV/dt	dVos/dt	5願し、50	kV/µs	V _{DS} ≤ 600V
Peak Diode Recovery dV/dt	dV/dt/500	ianin 925	kV/µs	Note *4
Peak Diode Recovery - di/dt	di/dt new OF-	100	A/µs	Note *5
Maximum Rower Dissingtion tú相設計(Crath		2.5	W	T₂=25°C
Maximum Fower Dissipation (注:新Mum not USE the		390	vv	Tc=25°C
Maximum Power Dissipation (注:新規設計にはれた) Operating and Storage Temperature range	Tch	150	°C	
Operating and Storage reinperature range	T _{stg}	-55 to +150	°C	

Note *1 : Limited by maximum channel temperature. Note *2 : Tch ≤ 150°C, See Fig.1 and Fig.2 Note *3 : Starting Tch=25°C, IAs=5.7A, L=95.4mH, Vbb=60V, Rg=50Ω, See Fig.1 and Fig.2

EAs limited by maximum channel temperature and avalanche current. Note *4 : Ir ≤ -ID, -di/dt=100A/µs, VDs peak ≤ 600V, Tch ≤ 150°C.

Note *5 : IF \leq -ID, dV/dt=25kV/µs, VDs peak \leq 600V, T_{ch} \leq 150°C.

Electrical Characteristics at T_c=25°C (unless otherwise specified) Static Ratings

Parameter	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I₀=2mA V₀s=V₀s		3	4	5	V
Zero Gate Voltage Drain Current		V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	-μA
	IDSS	V _{DS} =480V V _{GS} =0V	T _{ch} =125°C	-	250	-	
Gate-Source Leakage Current	Igss	V _{GS} = ± 30V V _{DS} =0V		-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =23.5A V _{GS} =10V		-	0.062	0.074	Ω
Gate resistance	RG	f=1MHz, open drain		-	1.1	-	Ω

Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g _{fs}	I _D =23.5A V _{DS} =25V	17	35	-	S
Input Capacitance	Ciss	V _{DS} =400V	-	3600	-	
Output Capacitance	Coss	V _{GS} =0V	-	105	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	7.5	-	1
Effective output capacitance, energy related (Note *6)	Co(er)	V _{GS} =0V V _{DS} =0400V	-	275	-	pF
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{GS} =0V V _{DS} =0400V ID=constant	-	945	-	
Turn-On Time	t _{d(on)}	V _{DD} =400V, V _{GS} =10V - I _D =23.5A, R _G =13Ω - See Fig.3 and Fig.4 -	-	146	-	
Turn-On Time	tr		-	32	-	ns
Turn-Off Time	t _{d(off)}		-	169	-	
Turn-Off Time	tr		19	-		
Total Gate Charge	Q _G		-	127	-	
Gate-Source Charge	Q _{GS}		-	33	-	nC
Gate-Drain Charge	Q _{GD}	− V _{GS} =10V _ See Fig.5	-	55	-	
Drain-Source crossover Charge	Qsw		-	16	-	

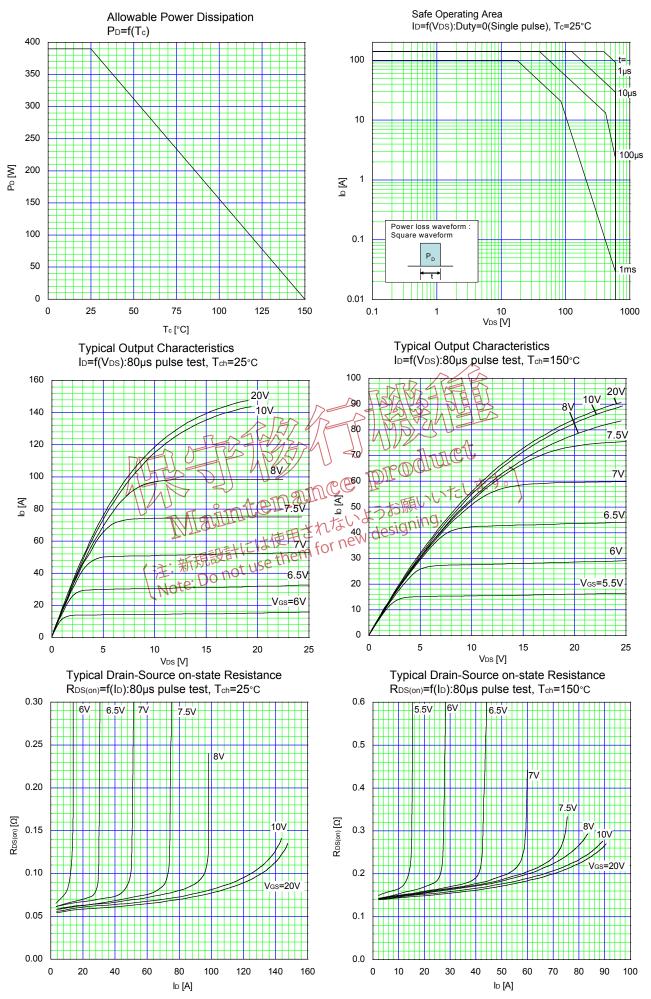
Note *6 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V. Note *7 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

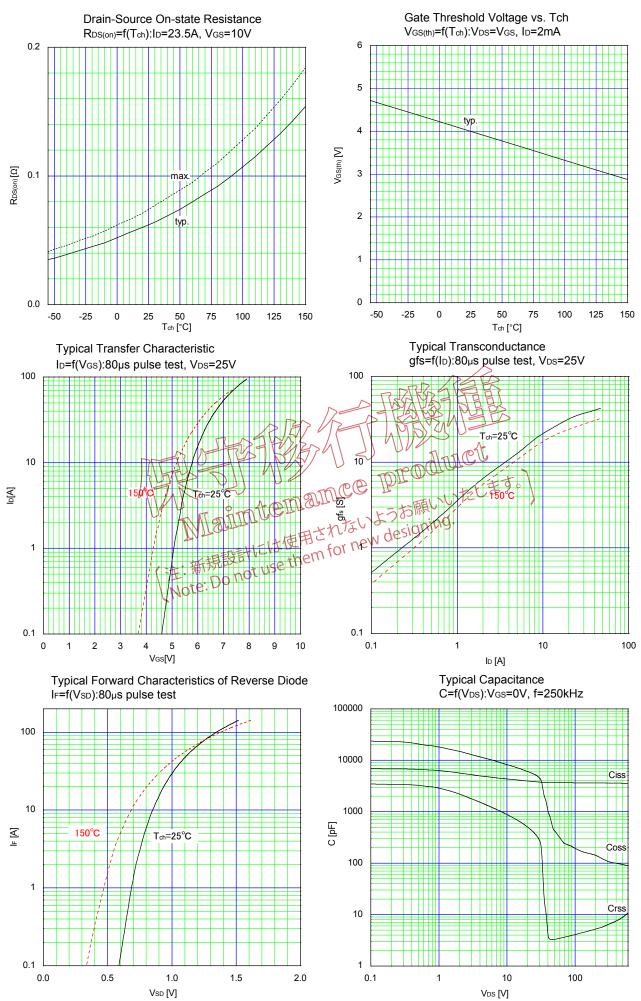
Reverse Diode

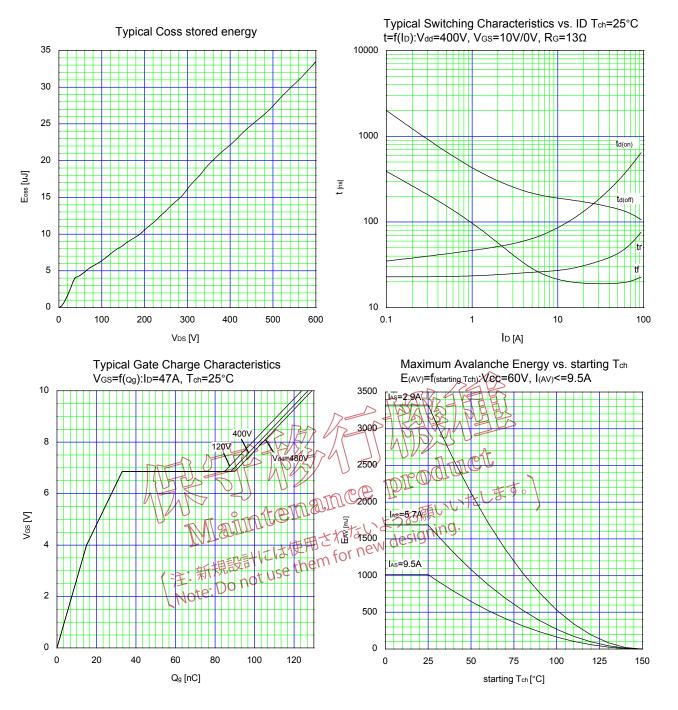
Parameter	Symbol	Conditions	e min.	typ.	max.	Unit
Avalanche Capability	IAV R	L=20.6mH, To=25°C See Fig. 7 and Fig.2	9.5	-	-	А
Diode Forward On-Voltage	THE S	h=47A,Vos=0V Ten=25°C	dituice	± 1.1	1.35	V
Reverse Recovery Time	t	The = 25 ℃ = The = 25 ℃ = To = 25 ℃ = 400V To = 25 ℃ = 400V See Fig.6 and Fig.7 for new design not use	NUTEL	210	-	ns
Reverse Recovery Charge	Q. MIGI	-di/dt=100A/usi されないる design	- 1119.	1.6	-	μC
Peak Reverse Recovery Current	泄:新規部	not USE	-	15	-	А

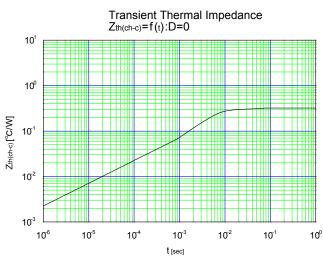
Thermal Resistance

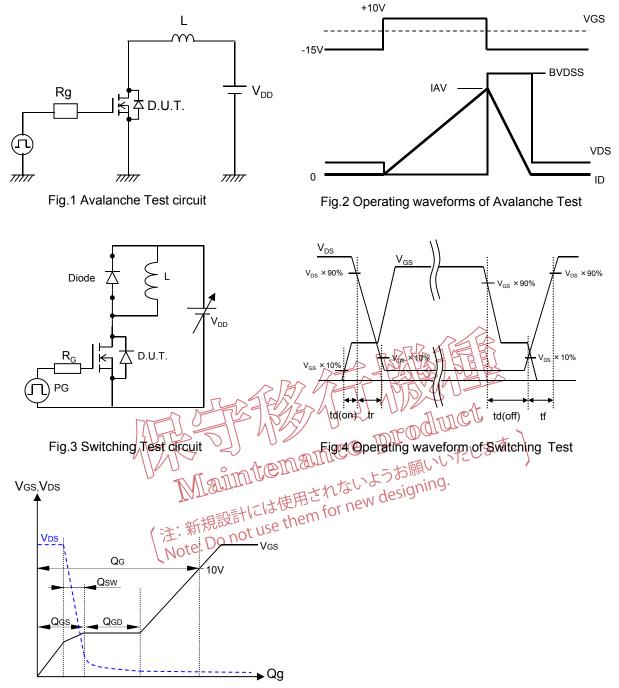
Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)	-	-	0.32	°C/W
Channel to Ambient	Rth(ch-a)	-	-	50	°C/W



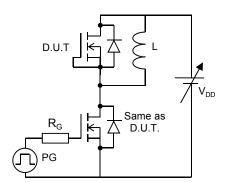












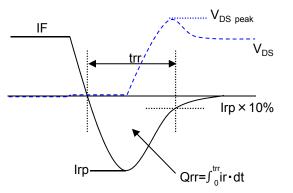
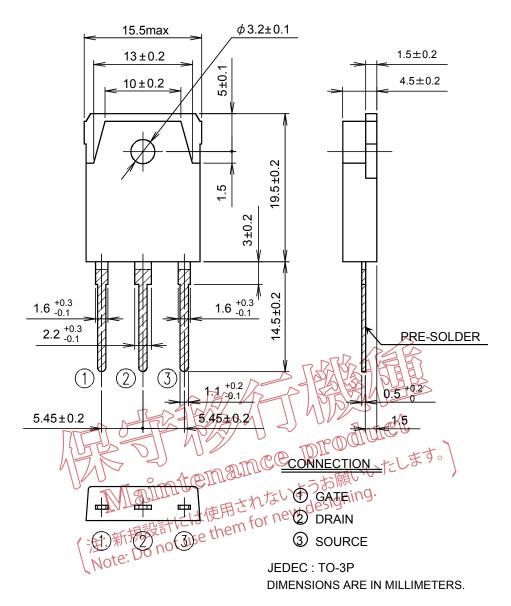


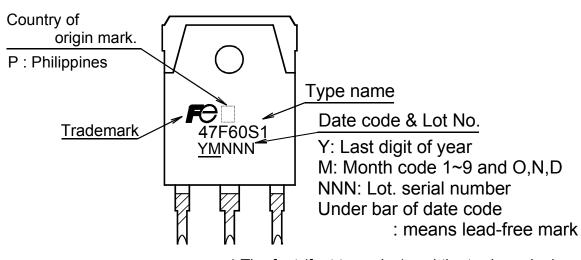
Fig.6 Reverse recovery Test circuit

Fig.7 Operating waveform of Reverse recovery Test

Outview: TO-3P Package



Marking



* The font (font type,size) and the trademark-size might be actually different.

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