

FMV20N60S1

Super J MOS[®] S1 series

N-Channel enhancement mode power MOSFET

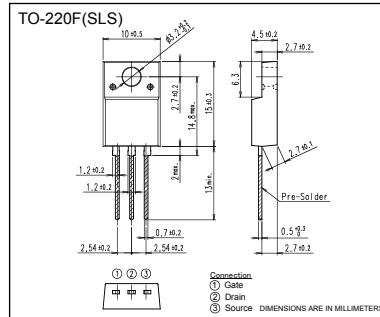
Features

- Pb-free lead terminal
- RoHS compliant

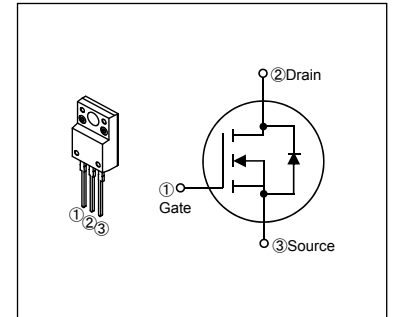
Applications

- For switching

Outline Drawings [mm]



Equivalent circuit schematic



Maximum Ratings and Characteristics

Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	600	V	
	V _{DSX}	600	V	V _{GS} =-30V
Continuous Drain Current	I _D	±20	A	T _c =25°C Note*1
		±12.6	A	T _c =100°C Note*1
Pulsed Drain Current	I _{DP}	±60	A	
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I _{AR}	6.6	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E _{AS}	472.2	mJ	Note *3
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	kV/μs	V _{DS} ≤600V
Peak Diode Recovery dV/dt	dV/dt	15	kV/μs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P _D	2.16	W	T _a =25°C
		53	W	T _c =25°C
Operating and Storage Temperature range	T _{ch}	150	°C	
	T _{stg}	-55 to +150	°C	
Isolation Voltage	V _{iso}	2	kVrms	t=60sec,f=60Hz

Note *1 : Limited by maximum channel temperature.
 Note *2 : T_{ch}≤150°C, See Fig.1 and Fig.2
 Note *3 : Starting T_{ch}=25°C, I_{AS}=2A, L=216mH, V_{DS}=60V, R_G=50Ω, See Fig.1 and Fig.2
 E_{AS} limited by maximum channel temperature and avalanche current.
 Note *4 : I_F≤-I_D, -di/dt=100A/μs, V_{DS}≤400V, T_{ch}≤150°C.
 Note *5 : I_F≤-I_D, dV/dt=15kV/μs, V_{DS}≤400V, T_{ch}≤150°C.

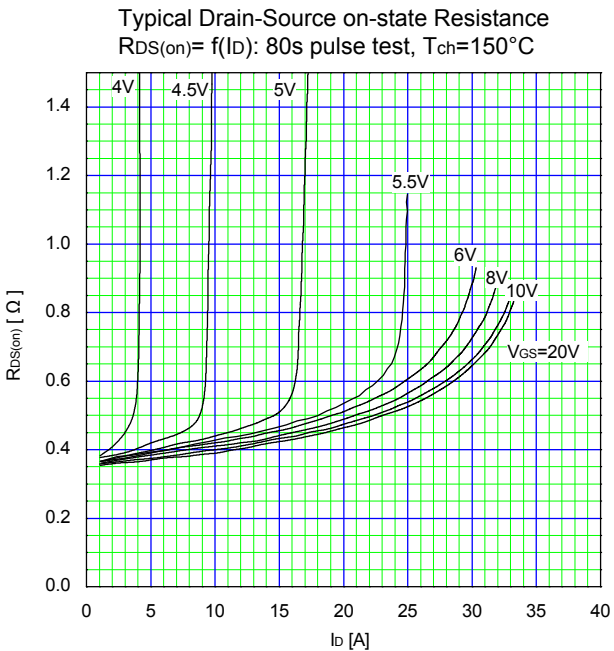
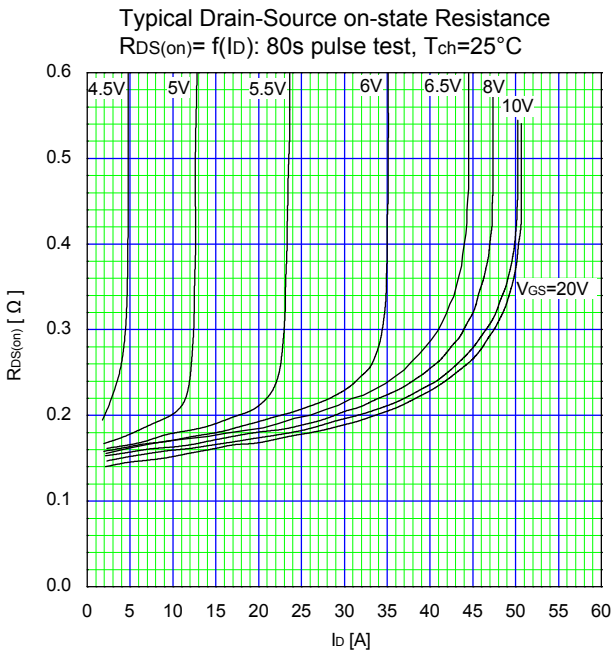
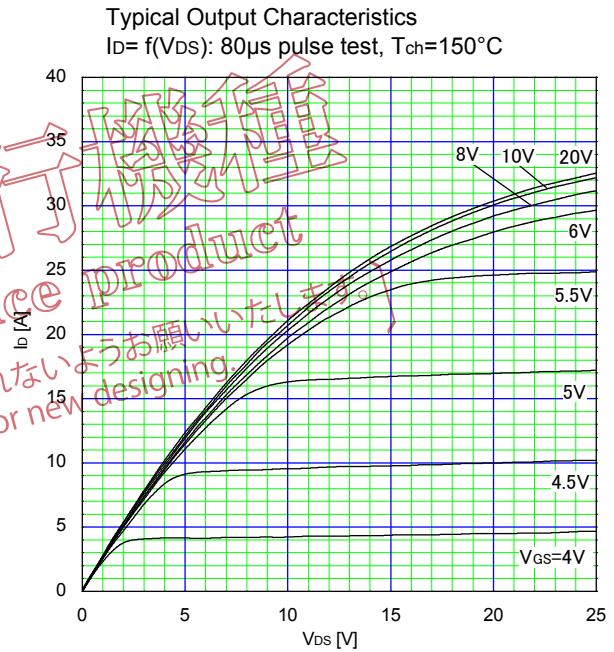
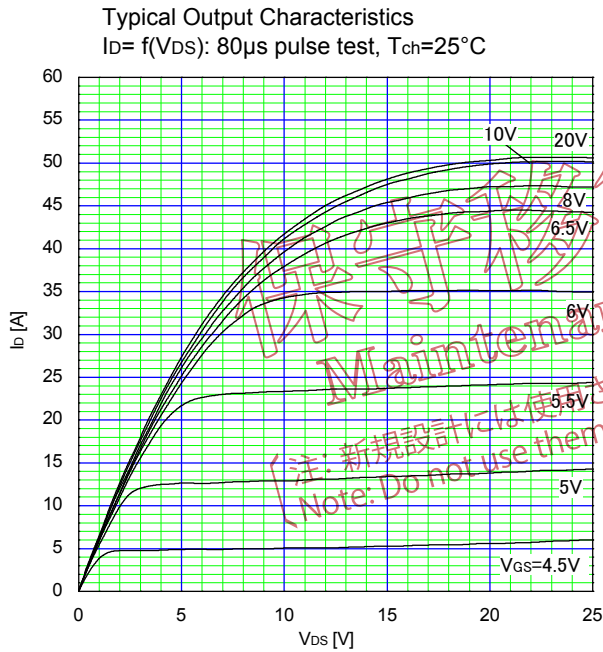
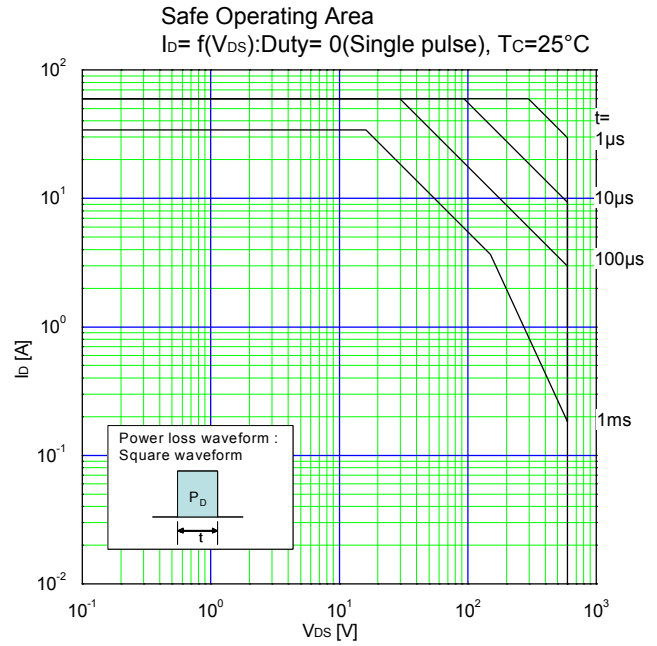
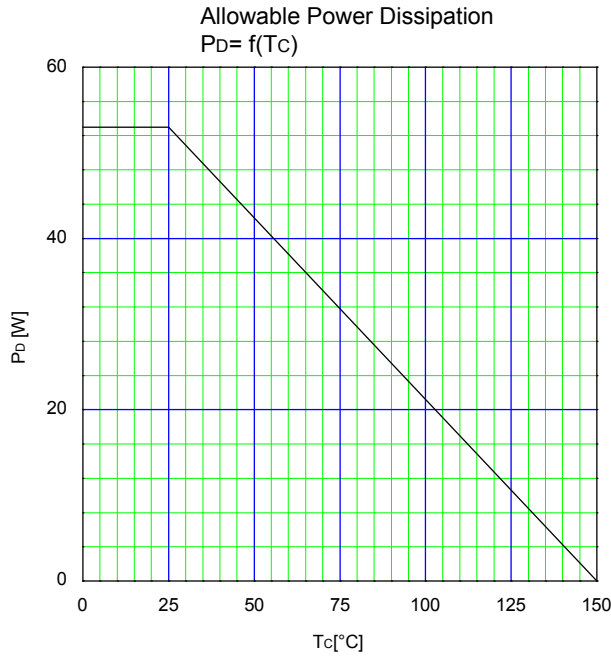
● Electrical Characteristics at T_c=25°C (unless otherwise specified)
Static Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V	600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =250μA V _{DS} =V _{GS}	2.5	3	3.5	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =600V V _{GS} =0V T _{ch} =25°C	-	-	25	μA
		V _{DS} =480V V _{GS} =0V T _{ch} =125°C	-	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ± 30V V _{DS} =0V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =10A V _{GS} =10V	-	0.161	0.19	Ω
Gate resistance	R _G	f=1MHz, open drain	-	3.7	-	Ω
Forward Transconductance	g _{fs}	I _D =10A V _{DS} =25V	8.5	17.5	-	S
Input Capacitance	C _{iss}	V _{DS} =10V	-	1470	-	pF
Output Capacitance	C _{oss}	V _{GS} =0V	-	3120	-	
Reverse Transfer Capacitance	C _{rss}	f=1MHz	-	280	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{GS} =0V V _{DS} =0...480V	-	90	-	
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{GS} =0V V _{DS} =0...480V I _D =constant	-	305	-	
Turn-On Time	t _{d(on)}	V _{DD} =400V, V _{GS} =10V I _D =10A, R _G =27Ω	-	22	-	ns
	t _r		-	40	-	
Turn-Off Time	t _{d(off)}	See Fig.3 and Fig.4	-	162	-	ns
	t _f		-	22	-	
Total Gate Charge	Q _G	V _{DD} =480V, I _D =20A	-	48	-	nC
Gate-Source Charge	Q _{GS}	V _{GS} =10V	-	12.5	-	
Gate-Drain Charge	Q _{GD}	See Fig.5	-	15	-	
Drain-Source crossover Charge	Q _{sw}		-	8	-	
Avalanche Capability	I _{AV}	L=6.02mH, T _{ch} =25°C See Fig.1 and Fig.2	6.6	-	-	A
Diode Forward On-Voltage	V _{SD}	I _r =20A, V _{GS} =0V T _{ch} =25°C	-	0.9	1.35	V
Reverse Recovery Time	t _{rr}	I _r =20A, V _{GS} =0V	-	370	-	ns
Reverse Recovery Charge	Q _{rr}	V _{DD} =400V -di/dt=100A/μs T _{ch} =25°C See Fig.6	-	6.2	-	μC
Peak Reverse Recovery Current	I _{rp}		-	32	-	A

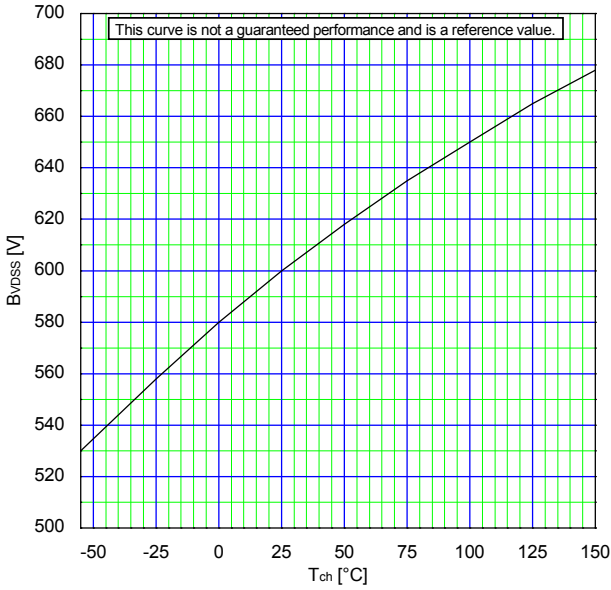
Note *6 : C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.
Note *7 : C_{o(tr)} is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.

● Thermal Characteristics

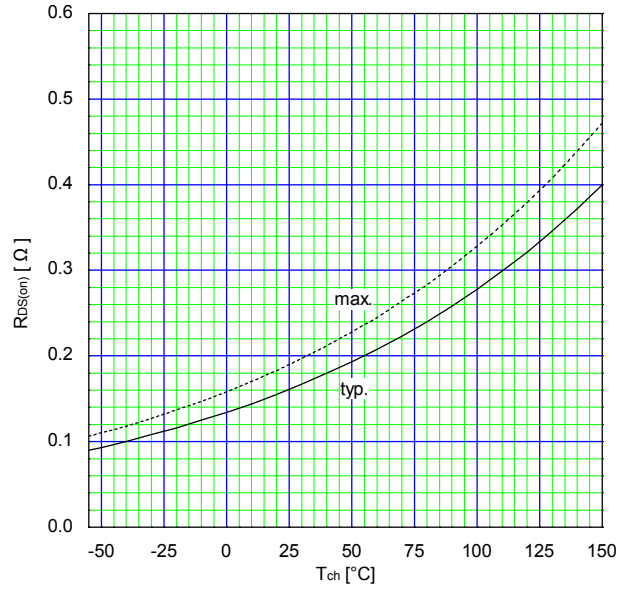
Description	Symbol	min.	typ.	max.	Unit
Channel to Case	R _{th(ch-c)}			2.36	°C/W
Channel to Ambient	R _{th(ch-a)}			58	°C/W



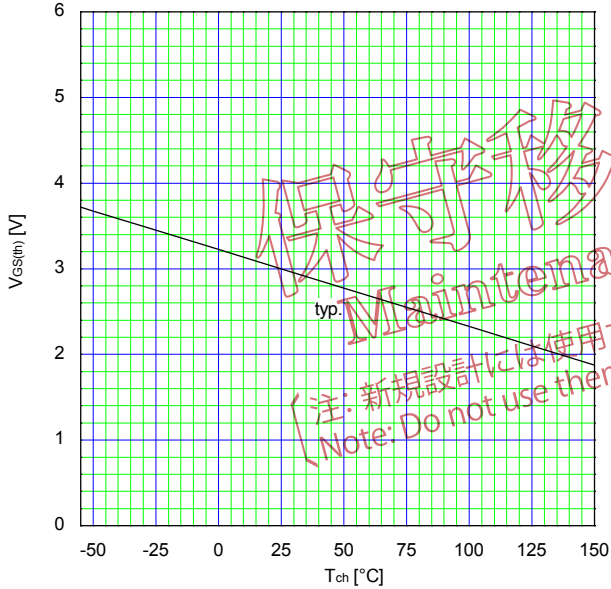
Drain-Source Breakdown Voltage
 $B_{VDS} = f(T_{ch})$: $I_D = 10\text{mA}$, $V_{GS} = 0\text{V}$



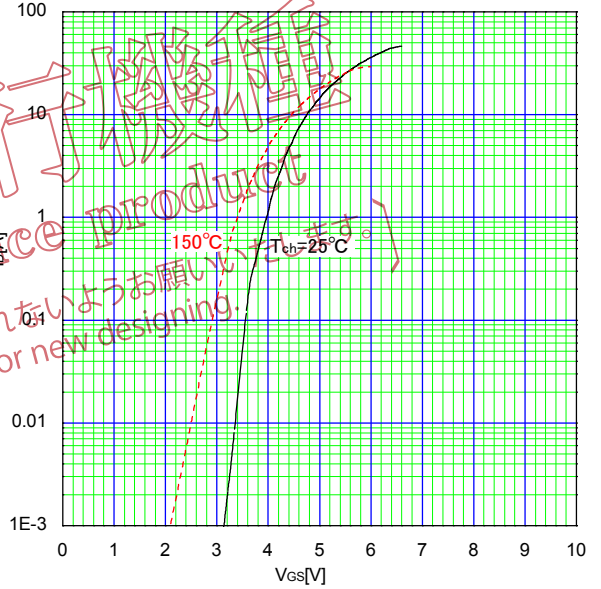
Drain-Source On-state Resistance
 $R_{DS(on)} = f(T_{ch})$: $I_D = 10\text{A}$, $V_{GS} = 10\text{V}$



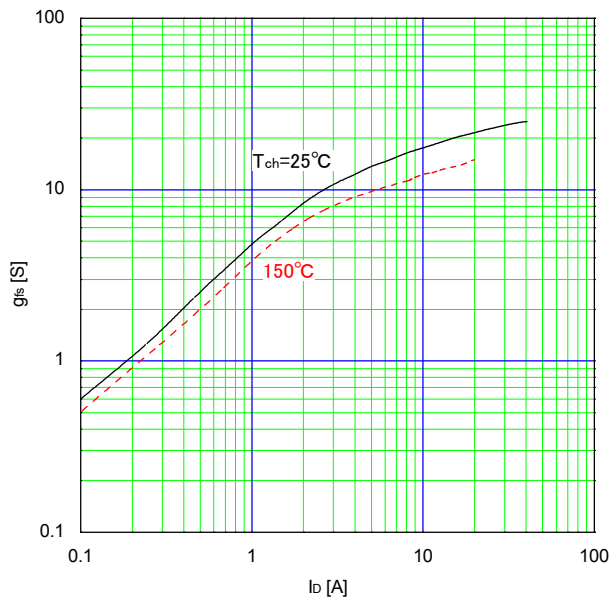
Gate Threshold Voltage vs. Tch
 $V_{GS(th)} = f(T_{ch})$: $V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$



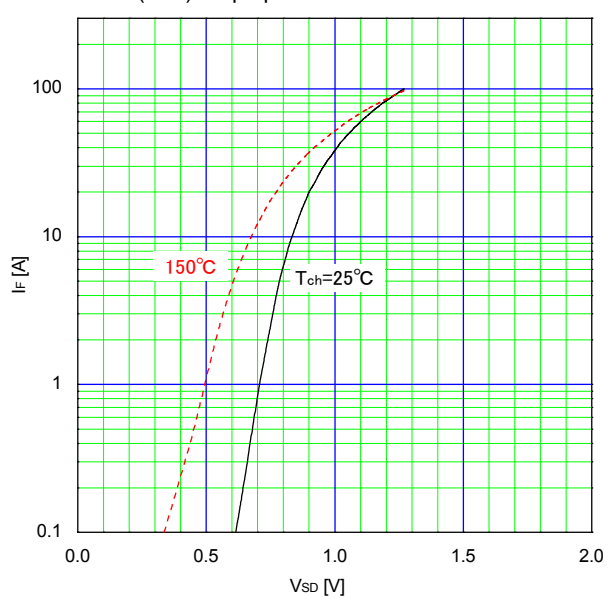
Typical Transfer Characteristic
 $I_D = f(V_{GS})$: 80μs pulse test, $V_{DS} = 25\text{V}$



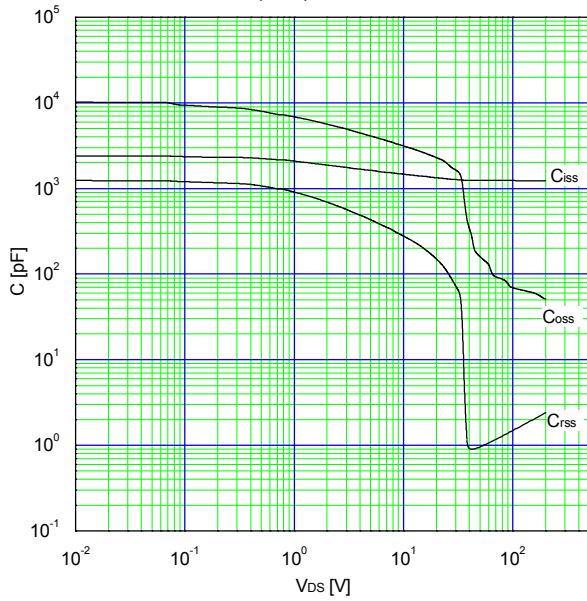
Typical Transconductance
 $g_{fs} = f(I_D)$: 80μs pulse test, $V_{DS} = 25\text{V}$



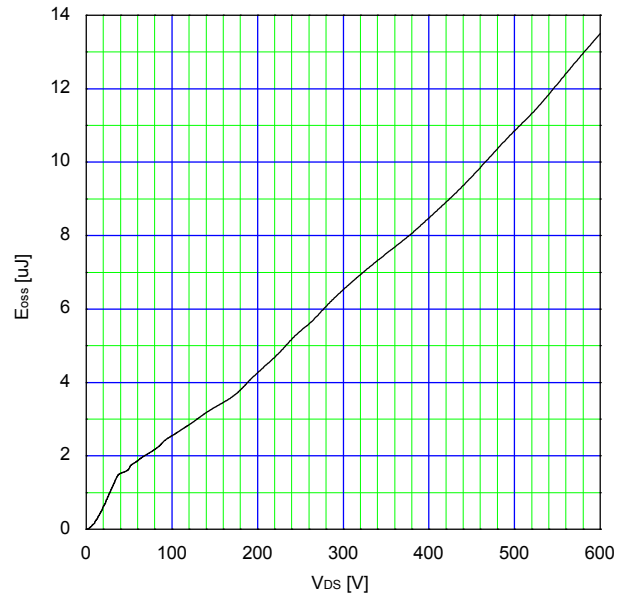
Typical Forward Characteristics of Reverse Diode
 $I_F = f(V_{SD})$: 80μs pulse test



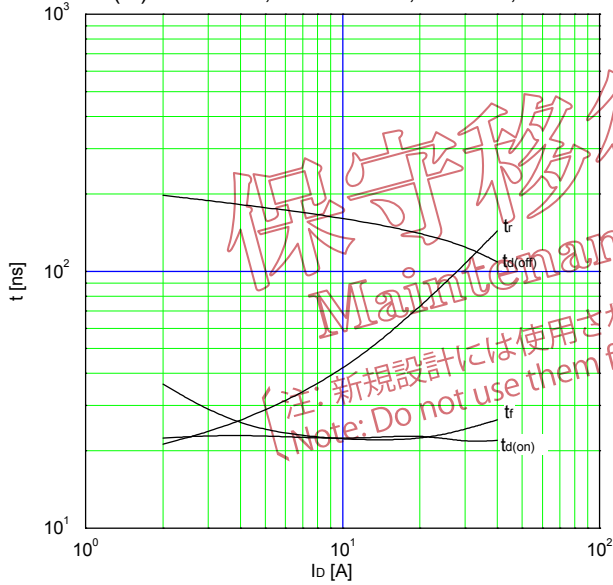
Typical Capacitance
 $C = f(V_{DS}): V_{GS}=0V, f=1MHz$



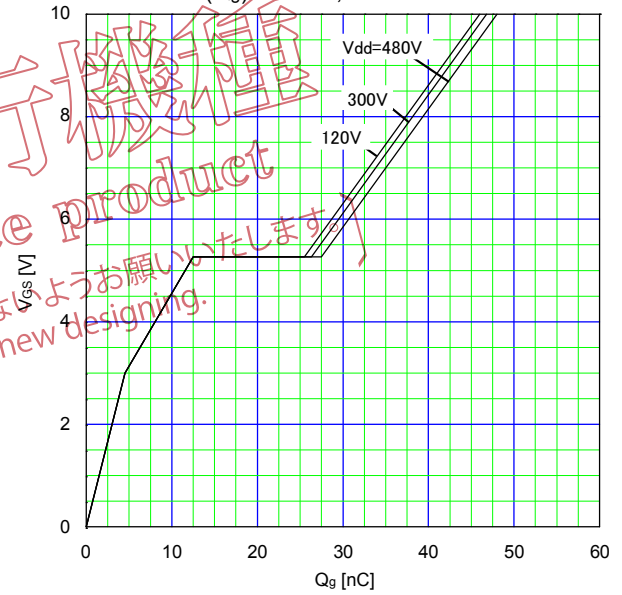
Typical Coss stored energy



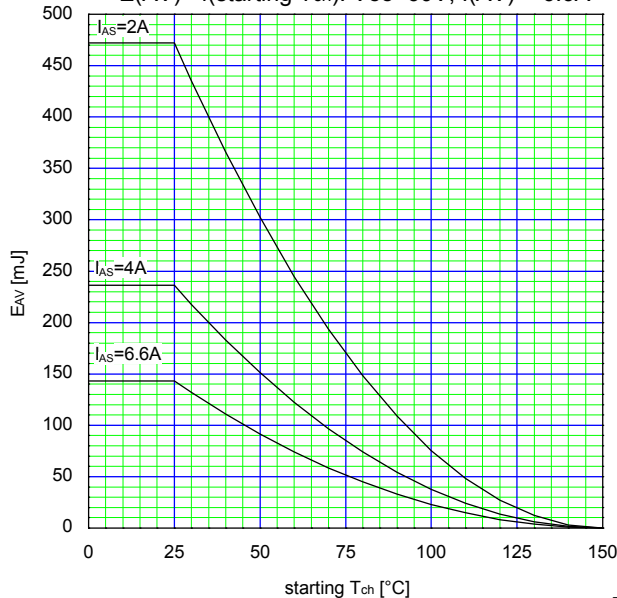
Typical Switching Characteristics vs. I_D $T_{ch}=25^\circ C$
 $t = f(I_D): V_{dd}=400V, V_{GS}=10V/0V, R_G=27\Omega, L=500uH$



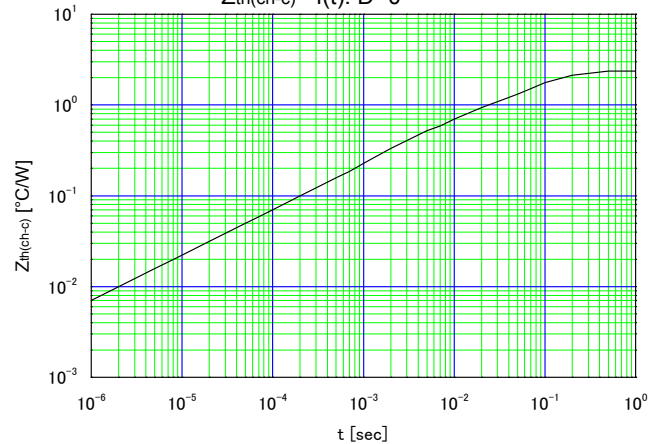
Typical Gate Charge Characteristics
 $V_{GS} = f(Q_g): I_D=20A, T_{ch}=25^\circ C$



Maximum Avalanche Energy vs. starting T_{ch}
 $E_{AV} = f(\text{starting } T_{ch}): V_{CC}=60V, I(AV) \le 6.6A$



Transient Thermal Impedance
 $Z_{th(ch-c)} = f(t): D=0$



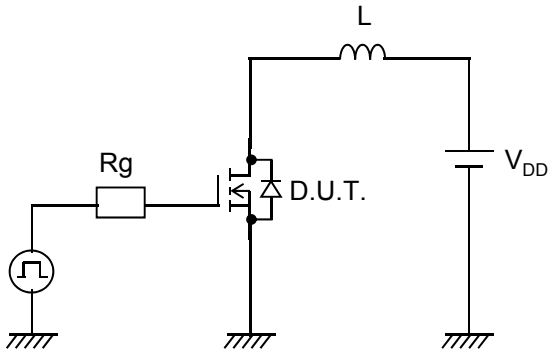


Fig.1 Avalanche Test circuit

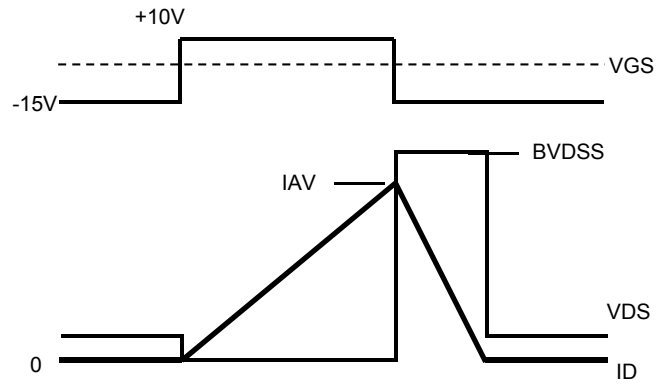


Fig.2 Operating waveforms of Avalanche Test

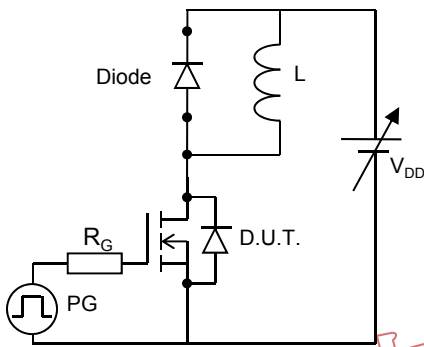


Fig.3 Switching Test circuit

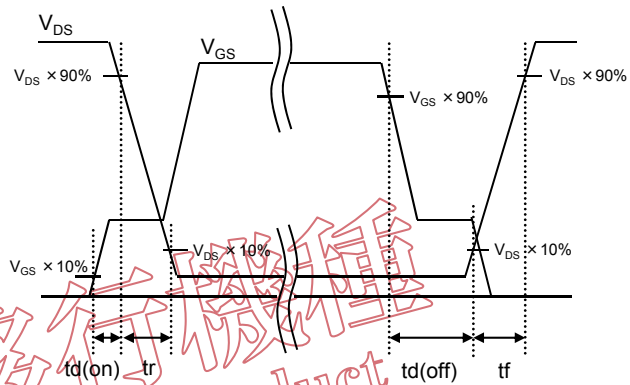


Fig.4 Operating waveform of Switching Test

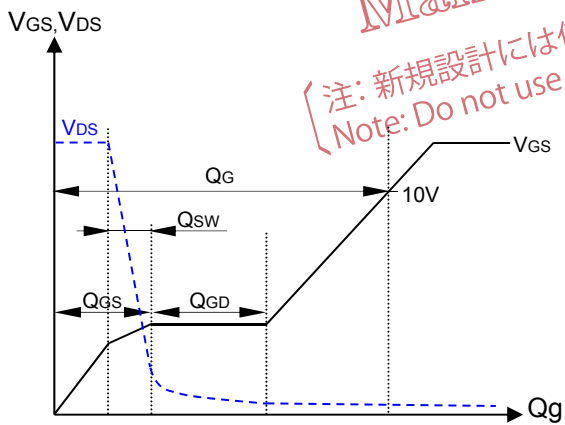


Fig.5 Operating waveform of Gate charge Test

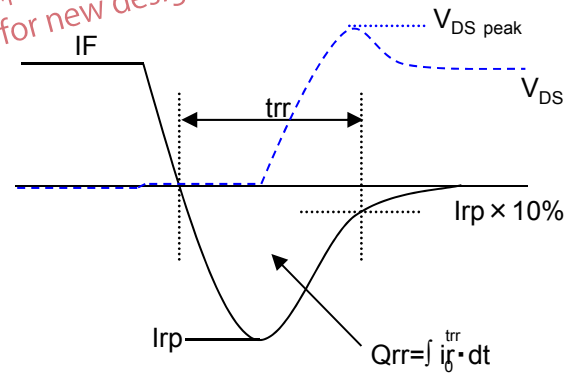
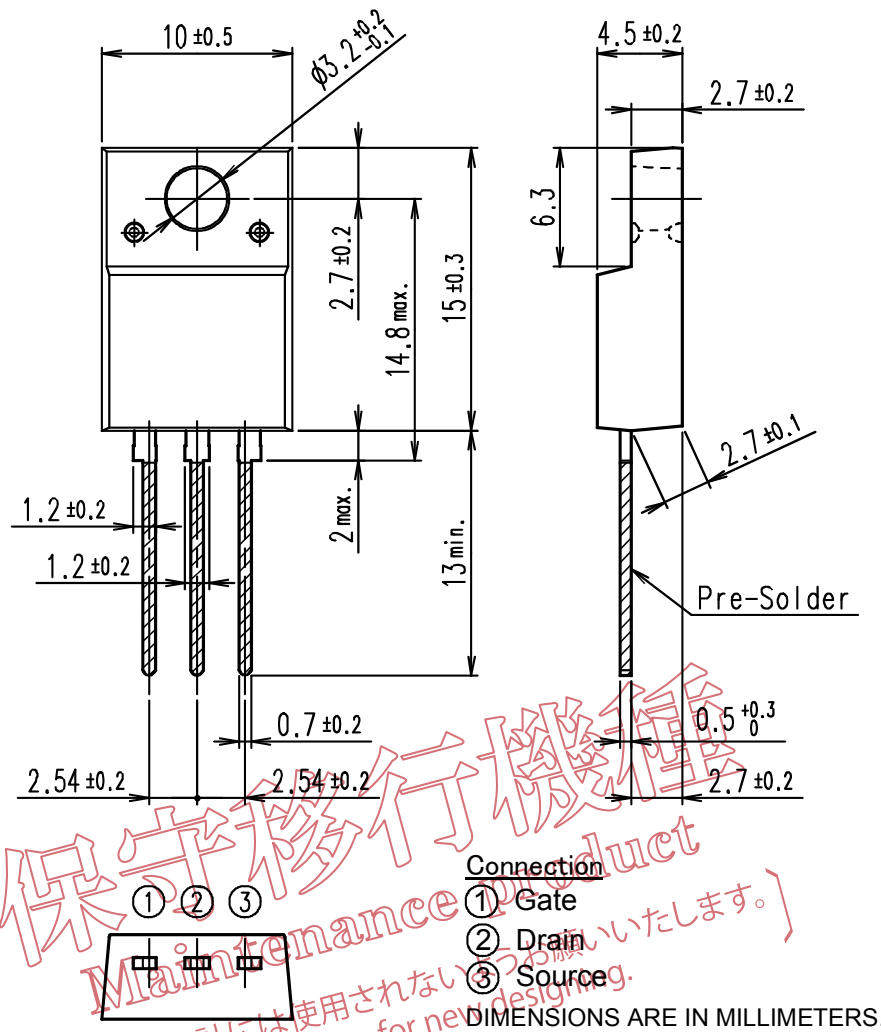


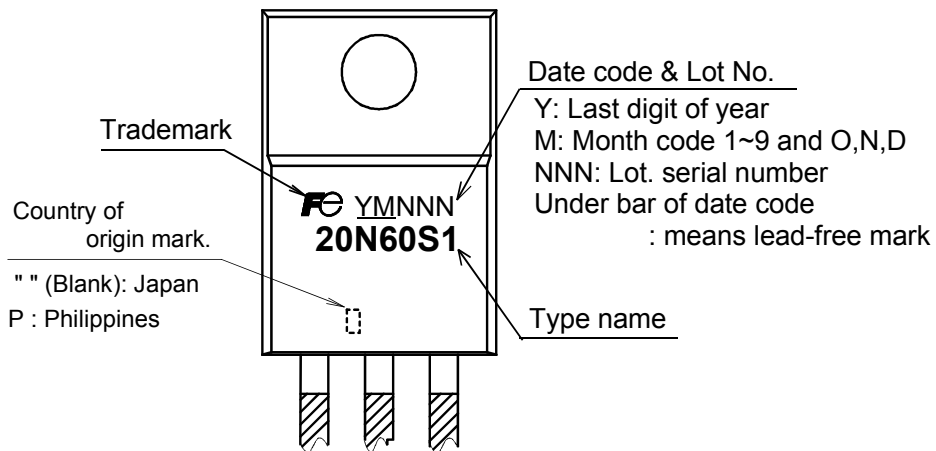
Fig.6 Operating waveform of Reverse recovery Test

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 Note: Do not use them for new designing.

■ Outview: TO-220F(SLS) Package



■ Marking



* The font (font type,size) and the trademark-size might be actually different.

WARNING

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