

FMV23N50ES

FUJI POWER MOSFET

Super FAP-E^{3S} series

N-CHANNEL SILICON POWER MOSFET

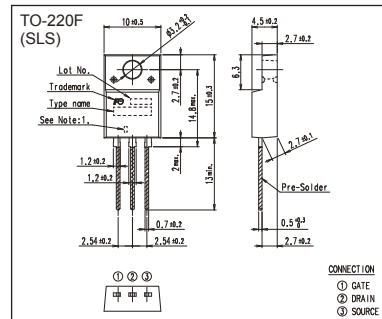
Features

- Maintains both low power loss and low noise
- Lower $R_{DS(on)}$ characteristic
- More controllable switching dv/dt by gate resistance
- Smaller V_{GS} ringing waveform during switching
- Narrow band of the gate threshold voltage ($4.2 \pm 0.5V$)
- High avalanche durability

Applications

- Switching regulators
- UPS (Uninterruptible Power Supply)
- DC-DC converters

Outline Drawings [mm]



Equivalent circuit schematic



Maximum Ratings and Characteristics

Absolute Maximum Ratings at $T_c=25^\circ C$ (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	500	V	
	V_{DSX}	500	V	$V_{GS} = -30V$
Continuous Drain Current	I_D	± 23	A	
Pulsed Drain Current	I_{DP}	± 92	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AS}	23	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	767.3	mJ	Note*2
Repetitive Maximum Avalanche Energy	E_{AR}	13	mJ	Note*3
Peak Diode Recovery dV/dt	dV/dt	5.4	kV/ μs	Note*4
Peak Diode Recovery $-di/dt$	$-di/dt$	100	A/ μs	Note*5
Maximum Power Dissipation	P_D	2.16	W	$T_a=25^\circ C$
		130		$T_c=25^\circ C$
Operating and Storage Temperature range	T_{ch}	150	$^\circ C$	
	T_{stg}	-55 to + 150	$^\circ C$	
Isolation Voltage	V_{ISO}	2	kVrms	$t = 60sec, f = 60Hz$

Electrical Characteristics at $T_c=25^\circ C$ (unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	500	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	3.7	4.2	4.7	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$	-	-	25	μA
		$V_{DS}=400V, V_{GS}=0V$	-	-	250	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=11.5A, V_{GS}=10V$	-	0.209	0.245	Ω
Forward Transconductance	g_{fs}	$I_D=11.5A, V_{DS}=25V$	8.5	17	-	S
Input Capacitance	C_{iss}	$V_{DS}=25V$	-	2700	4050	pF
Output Capacitance	C_{oss}	$V_{GS}=0V$	-	330	495	
Reverse Transfer Capacitance	C_{rss}	$f=1MHz$	-	20	30	
Turn-On Time	$t_d(on)$	$V_{cc}=300V$	-	42	63	ns
	t_r	$V_{GS}=10V$	-	36	54	
Turn-Off Time	$t_d(off)$	$I_D=11.5A$	-	94	141	
	t_f	$R_{GS}=10\Omega$	-	17	25.5	
Total Gate Charge	Q_G	$V_{cc}=250V$	-	73	109.5	nC
Gate-Source Charge	Q_{GS}	$I_D=23A$	-	24	36	
Gate-Drain Charge	Q_{GD}	$V_{GS}=10V$	-	27	40.5	
Gate-Drain Crossover Charge	Q_{SW}		-	10	15	
Avalanche Capability	I_{AV}	$L=1.16mH, T_{ch}=25^\circ C$	23	-	-	A
Diode Forward On-Voltage	V_{SD}	$I_F=23A, V_{GS}=0V, T_{ch}=25^\circ C$	-	0.90	1.35	V
Reverse Recovery Time	t_{rr}	$I_F=23A, V_{GS}=0V$	-	0.5	-	μs
Reverse Recovery Charge	Q_{rr}	$-di/dt=100A/\mu s, T_{ch}=25^\circ C$	-	8.0	-	μC

Thermal Characteristics

Description	Symbol	Test Conditions	min.	typ.	max.	Unit
Thermal resistance	$R_{th(ch-c)}$	Channel to Case			0.960	$^\circ C/W$
	$R_{th(ch-a)}$	Channel to Ambient			58.0	$^\circ C/W$

Note *1 : $T_{ch} \leq 150^\circ C$.

Note *2 : Stating $T_{ch}=25^\circ C, I_{AS}=10A, L=14.1mH, V_{cc}=50V, R_G=50\Omega$.

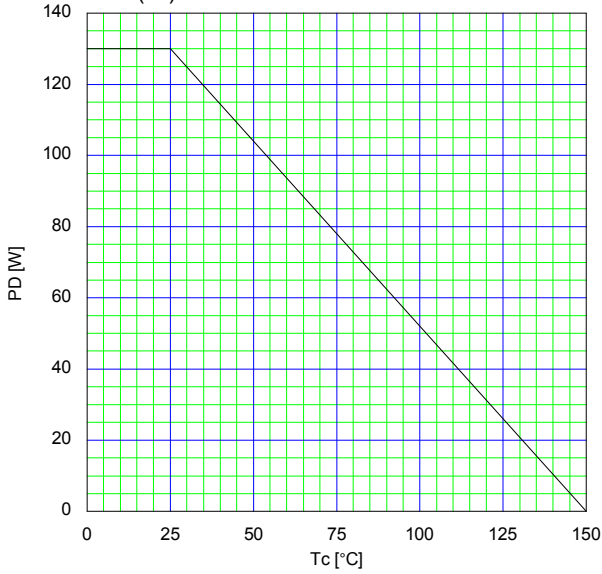
E_{AS} limited by maximum channel temperature and avalanche current.
See to 'Avalanche Energy' graph.

Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.
See to the 'Transient Thermal impedance' graph.

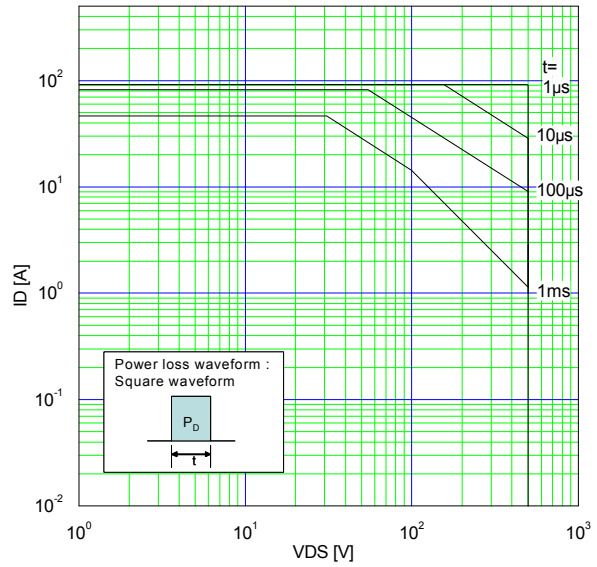
Note *4 : $I_{FS}=I_D, -di/dt=100A/\mu s, V_{ccs}=BV_{DSS}, T_{ch}=150^\circ C$.

Note *5 : $I_{FS}=I_D, dv/dt=5.4kV/\mu s, V_{ccs}=BV_{DSS}, T_{ch}=150^\circ C$.

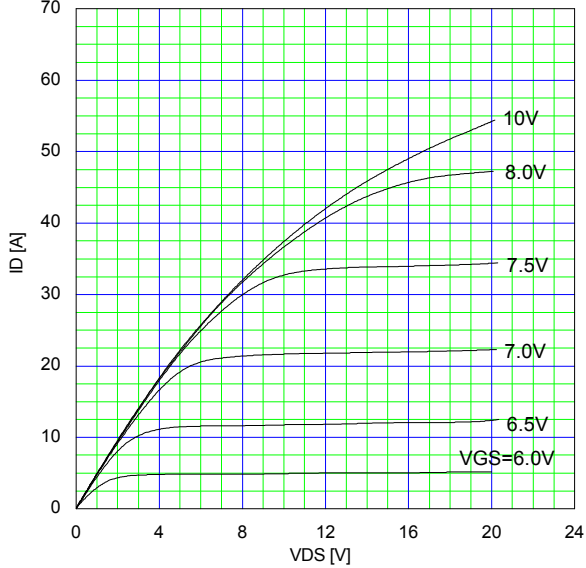
Allowable Power Dissipation
 $P_D = f(T_c)$



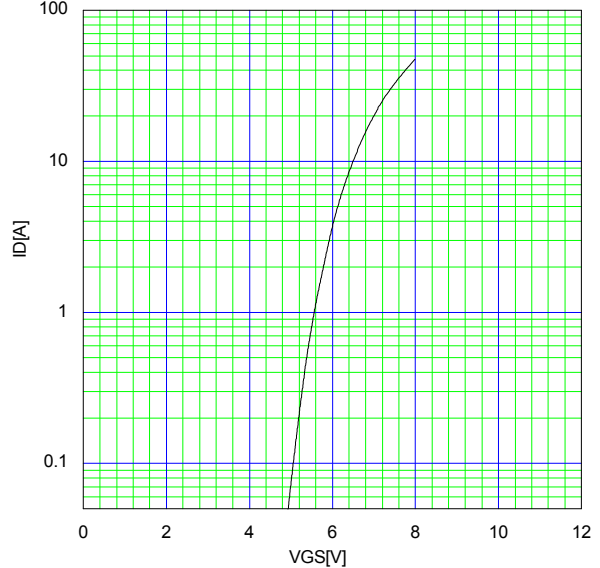
Safe Operating Area
 $I_D = f(V_{DS})$; Duty=0 (Single pulse), Tc=25 °C



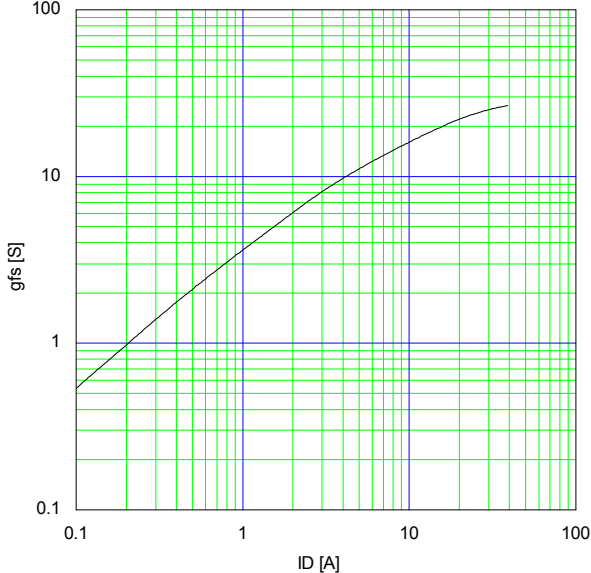
Typical Output Characteristics
 $I_D = f(V_{DS})$; 80 μs pulse test, Tch=25 °C



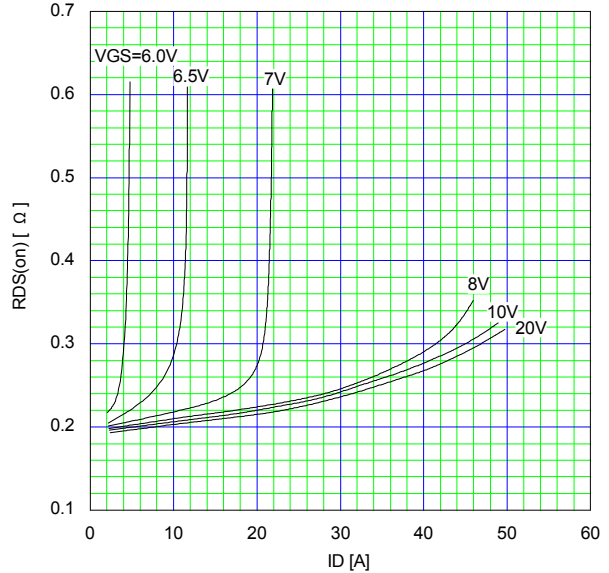
Typical Transfer Characteristic
 $I_D = f(V_{GS})$; 80 μs pulse test, VDS=25V, Tch=25 °C



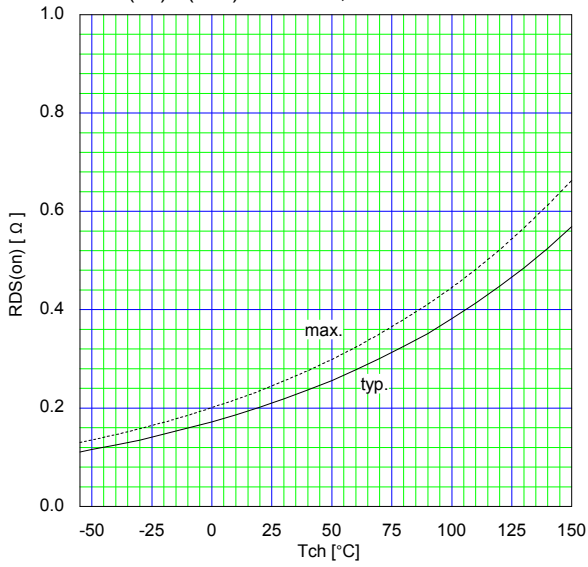
Typical Transconductance
 $g_{fs} = f(I_D)$; 80 μs pulse test, VDS=25V, Tch=25 °C



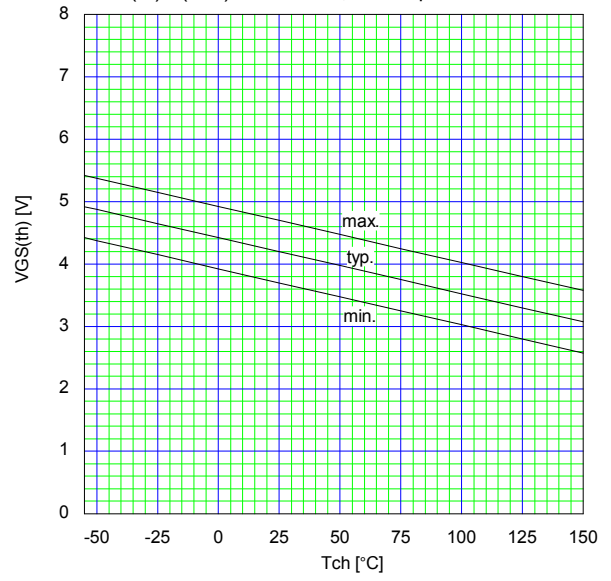
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$; 80 μs pulse test, Tch=25 °C



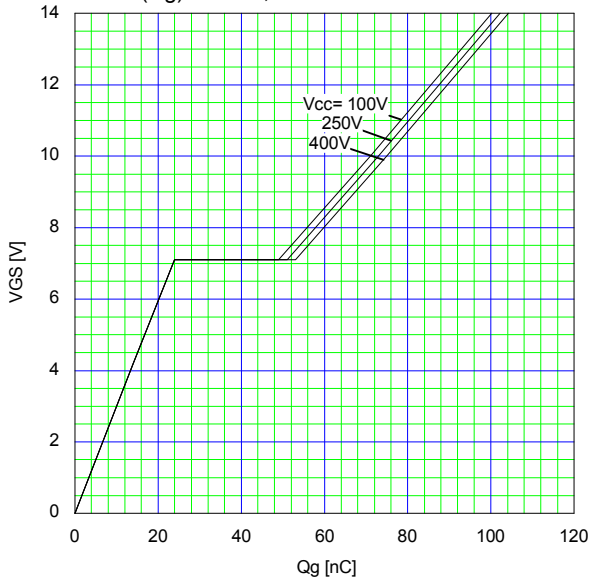
Drain-Source On-state Resistance
 $R_{DS(on)} = f(T_{ch})$; $I_D = 11.5A, V_{GS} = 10V$



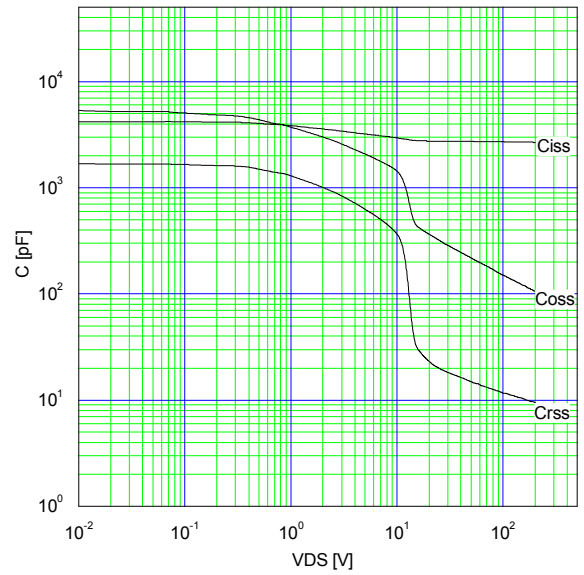
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)} = f(T_{ch})$; $V_{DS} = V_{GS}, I_D = 250\mu A$



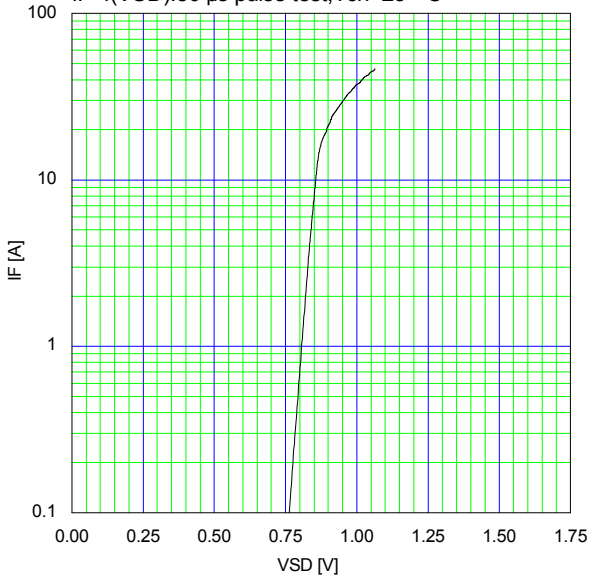
Typical Gate Charge Characteristics
 $V_{GS} = f(Q_g)$; $I_D = 23A, T_{ch} = 25^\circ C$



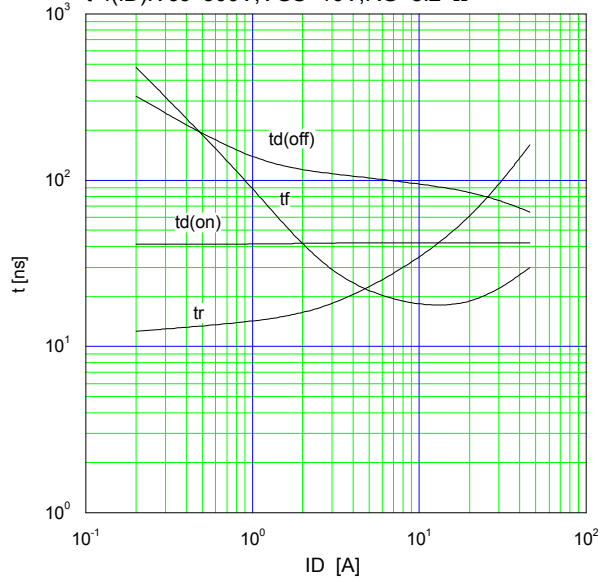
Typical Capacitance
 $C = f(V_{DS})$; $V_{GS} = 0V, f = 1MHz$



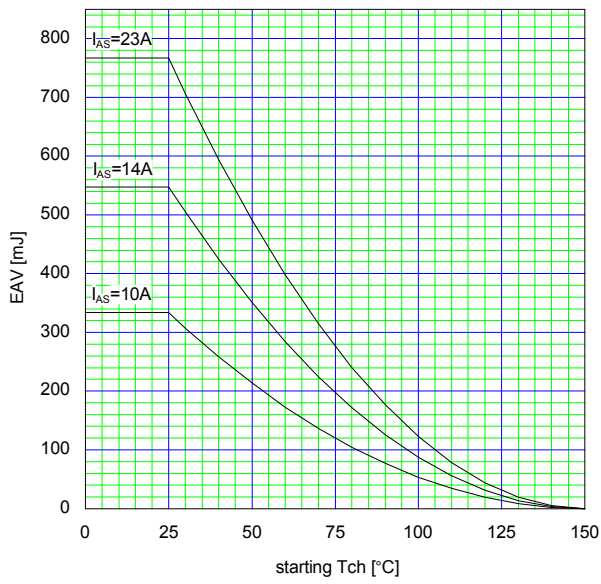
Typical Forward Characteristics of Reverse Diode
 $I_F = f(V_{SD})$; $80\mu s$ pulse test, $T_{ch} = 25^\circ C$



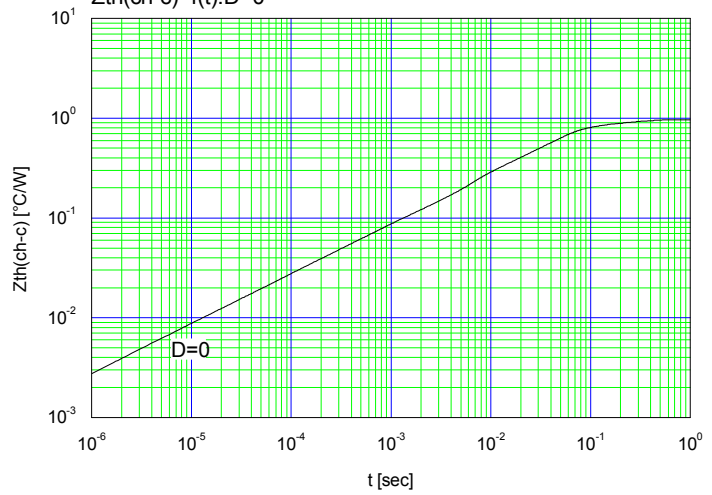
Typical Switching Characteristics vs. I_D
 $t = f(I_D)$; $V_{cc} = 300V, V_{GS} = 10V, R_G = 8.2\ \Omega$



Maximum Avalanche Energy vs. starting Tch
 $E(AV)=f(\text{starting Tch}):V_{CC}=50V, I(AV)\leq 23A$



Maximum Transient Thermal Impedance
 $Z_{th}(ch-c)=f(t):D=0$



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