

MOSFET – Power, N-Channel, SUPERFET[®] III, Easy Drive

650 V, 24 A, 125 mΩ

FCPF125N65S3

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

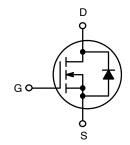
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 105 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 44 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 405 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

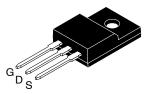
Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	125 mΩ @ 10 V	24 A



POWER MOSFET



TO-220F CASE 221AT

MARKING DIAGRAM



\$Y = onsemi Logo &Z = Assembly Plant Code &3 = Data Code (Year & Week)

&K = Lot

FCPF125N65S3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$, Unless otherwise noted)

Symbol	Parameter	Value	Unit		
V_{DSS}	Drain to Source Voltage	650	V		
V_{GSS}	Gate to Source Voltage	- DC	±30	V	
		– AC (f > 1 Hz)	±30		
I _D	Drain Current – Continuous (T _C = 25°C)		24*	Α	
		– Continuous (T _C = 100°C)	15*		
I _{DM}	Drain Current	- Pulsed (Note 1)	60*	Α	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	115	mJ		
I _{AS}	Avalanche Current (Note 2)	3.7	Α		
E _{AR}	Repetitive Avalanche Energy (Note 1)	0.38	mJ		
dv/dt	MOSFET dv/dt	100	V/ns		
	Peak Diode Recovery dv/dt (Note 3)		20		
P_{D}	Power Dissipation	(T _C = 25°C)	38	W	
		- Derate Above 25°C	0.31	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C		
TL	Maximum Lead Temperature for Soldering, 1/8"	300	°C		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.	3.24	°C/W
$R_{\theta JA}$	R _{0JA} Thermal Resistance, Junction to Ambient, Max.		

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF125N65S3	FCPF125N65S3	TO-220F	Tube	N/A	N/A	50 Units

^{1.} Repetitive rating: pulse–width limited by maximum junction temperature. 2. $I_{AS} = 3.7 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 12 \text{ A}$, $di/dt \le 200 \text{ A/µs}$, $V_{DD} \le 400 \text{ V}$, starting $T_J = 25^{\circ}\text{C}$.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
OFF CHARACT	ERISTICS		•			
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		0.65		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 520 V, T _C = 125°C		1.35		
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
ON CHARACTE	RISTICS					
V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.54 mA	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A		105	125	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 12 A		16		S
DYNAMIC CHAI	RACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1790		pF
C _{oss}	Output Capacitance			40		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		405		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		60		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 12 A, V _{GS} = 10 V		44		nC
Q_{gs}	Gate to Source Gate Charge	(Note 4)		12		nC
$Q_{\sf gd}$	Gate to Drain "Miller" Charge			19		nC
ESR	Equivalent Series Resistance	f = 1 MHz		4		Ω
SWITCHING CH	IARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 12 \text{ A}, V_{GS} = 10 \text{ V},$		22		ns
t _r	Turn-On Rise Time	$R_g = 4.7 \Omega$ (Note 4)		25		ns
t _{d(off)}	Turn-Off Delay Time			60		ns
t _f	Turn-Off Fall Time			15		ns
SOURCE-DRAII	N DIODE CHARACTERISTICS					
I _S	Maximum Continuous Source to Drain Diode Forward Current				24	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current				60	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 12 A,		362		ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs		6.36		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

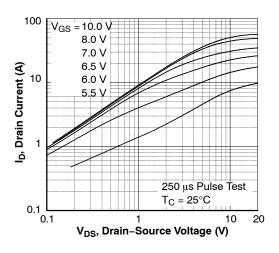


Figure 1. On-Region Characteristics

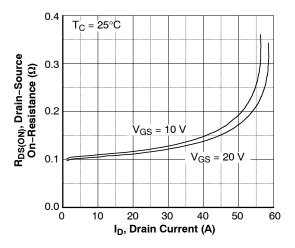


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

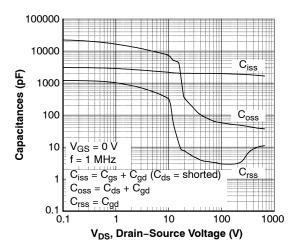


Figure 5. Capacitance Characteristics

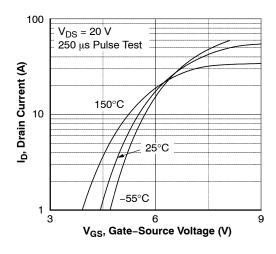


Figure 2. Transfer Characteristics

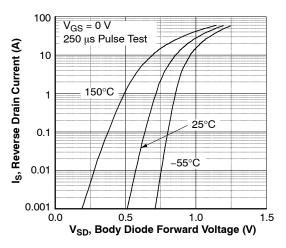


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

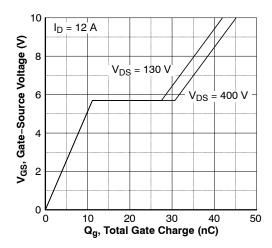


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

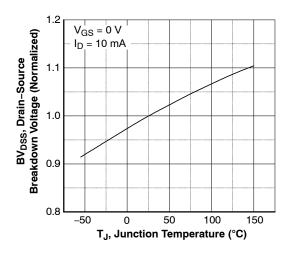


Figure 7. Breakdown Voltage Variation vs. Temperature

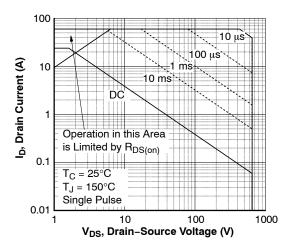


Figure 9. Maximum Safe Operating Area

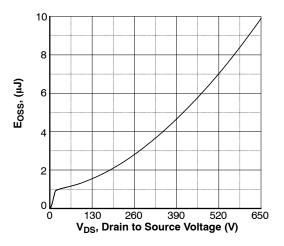


Figure 11. $E_{\mbox{OSS}}$ vs. Drain to Source Voltage

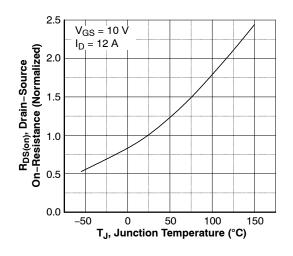


Figure 8. On–Resistance Variation vs. Temperature

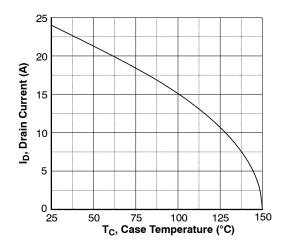


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

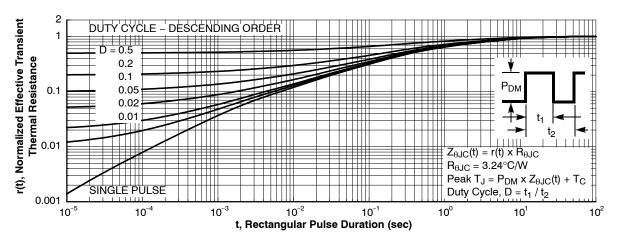


Figure 12. Transient Thermal Response Curve

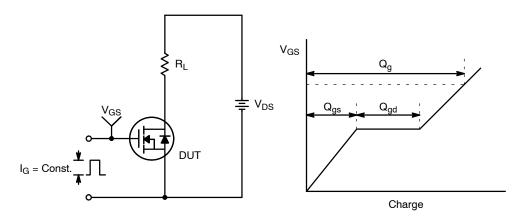


Figure 13. Gate Charge Test Circuit & Waveform

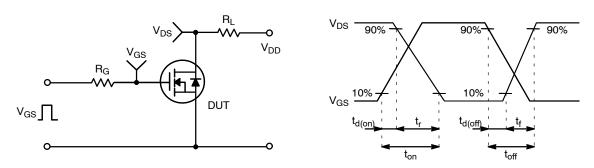


Figure 14. Resistive Switching Test Circuit & Waveforms

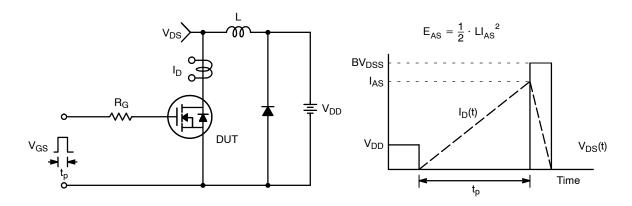


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

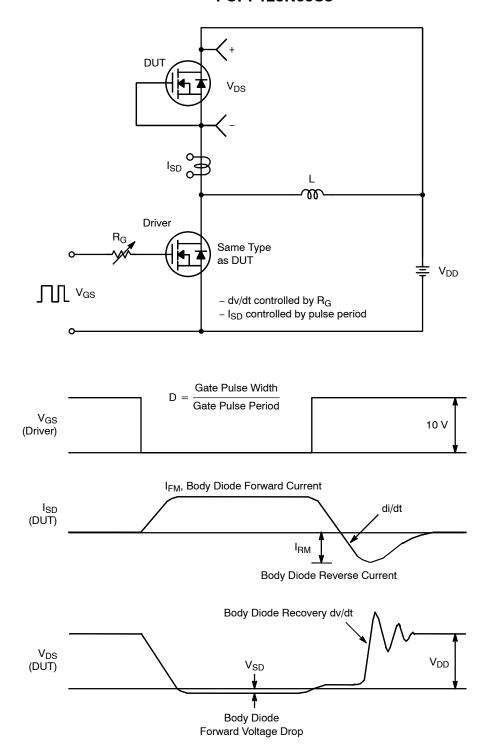
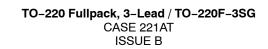
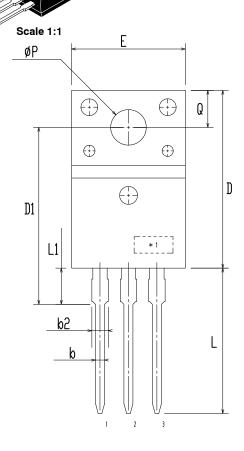


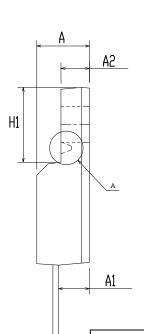
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

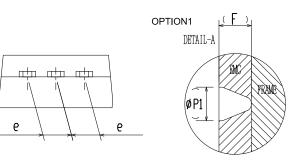
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DATE 19 JAN 2021







DIM	MILLIMITERS				
ויונע	MIN NDM M		MAX		
Α	4.50	4.70	4.90		
A1	2.56	2.76	2.96		
A2	2.34	2.54	2.74		
b	0.70	0.80	0.90		
b2	~	2	1.47		
С	0.45	0.50	0.60		
D	15.67 15.87		16.07		
D1	15.60	15.80	16.00		
E	9.96	10.16	10.36		
е	2.34	2.54	2.74		
F	~	0.84	2		
H1	6.48	6.68	6.88		
L	12.78	12.98	13.18		
L1	3.03	3.23	3.43		
ØΡ	2.98	3.18	3.38		
Ø P1	~	1.00	~		
Q	3.20	3.30	3.40		

MILLIMITEDS

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.

C

C. OPTION 1 - WITH SUPPORT PIN HOLE OPTION 2 - NO SUPPORT PIN HOLE

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