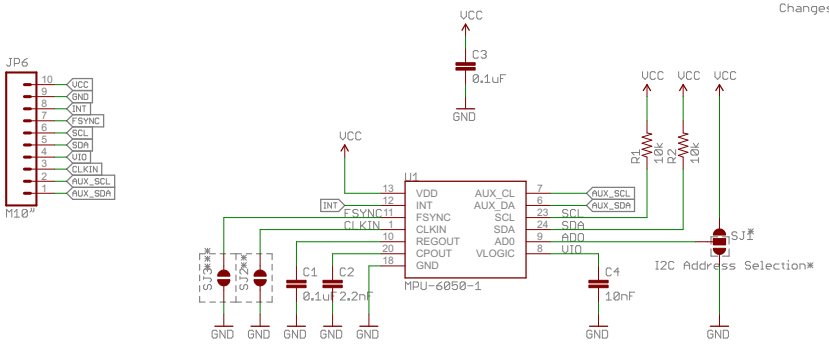

Changes to V11
SCL and SDA were switched on V10, fixed on V11
Broke out VLOGIC line
C2 was mislabled as 10nF, should have been 2.2nF.
Added selectable jumpers to CLK, FSYNC and AD0
Minor layout changes
Played around with IC footprint.
Added 4 small tcream squares to middle pad.
Rounded and elongated pads.

BOM changes
YES
C2 is now 2.2nF instead of 10nF

New Stencil
YES

Changes to V12:

* Two MPU-60X0s can be connected to the same I2C bus
The LSB bit of the 7 bit address is determined by the logic level on pin AD0.
Default Address = 0x68 (pin AD0 is logic low)
Alternative Address =0x69 (pin AD0 is logic high)

** Optional external reference clock input. Connected to GND by default.
Cut trace for external clock

*** Frame synchronization digital input. Connected to GND by default
Cut trace for external sync

open hardware

TITLE: Triple_Axis_Accelerometer_-_Gyro_Breakout_-_MPU-6050

Design by: J. Bartlett	REV: v12
Revision By: E. Orosel	
Date: 7/23/2013 3:47:34 PM	Sheet: 1/1