

Innovating Energy Technology

http://www.fujielectric.com/products/semiconductor/ **FUJI POWER MOSFET**

Super J MOS[®] S2 series

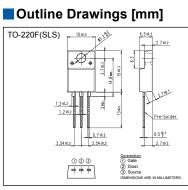
N-Channel enhancement mode power MOSFET

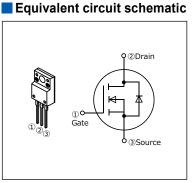
Features

Pb-free lead terminal **RoHS** compliant uses Halogen-free molding compound

Applications

For switching





Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain Source Veltere	V _{DS}	600	V	
Drain-Source Voltage	VDSX	600	V	V _{GS} =-30V
Continuous Drain Current	I _D	20	А	Tc=25°C Note*1,2
		12.6	А	Tc=100°C Note*1,2
Pulsed Drain Current	I _{DP}	62	А	Note *2
Gate-Source Voltage	V _{GS}	±30	V	
Non-Repetitive Maximum Avalanche Current	las	2.3	А	Note *3
Non-Repetitive Maximum Avalanche Energy	Eas	559	mJ	Note *4
Maximum Drain-Source dV/dt	dV _{DS} /dt	50	V/ns	V _{DS} ≤ 600V
Continuous	1	20	А	Tc=25°C Note*1,2
Diode Forward Current	/sd	12.6	А	Tc=100°C Note*1,2
Pulsed Diode Forward Current	ISDP	62	А	Note *2
Peak Diode Recovery dV/dt	dV/dt	15	V/ns	Note *5
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *6
Mewimeum Deuven Dissingéis n		2.16	14/	<i>T</i> ₂=25°C
Maximum Power Dissipation	PD	38	W	<i>T</i> c=25°C
Operating and Starsen Temperature range	Tch	150	°C	
Operating and Storage Temperature range	T _{stg}	-55 to +150	°C	
Isolation Voltage (TO-220F)	Viso	2	kVrms	t=60sec, f=60Hz

Note *1 : Maximum duty cycle D=0.6 Note *2 : Limited by maximum channel temperature. Note *3 : *T*ei≤150°C, See Fig.1 and Fig.2 Note *4 : Starting *T*ei=25°C, *I*As=1.4A, L=559mH, *V*ob=60V, *R*c=50Ω, See Fig.1 and Fig.2 Eas limited by maximum channel temperature and avalanche current.

Note *5 : Iso≤15.5A, -ididt≤100A/µs, Vos peak≤600V, T₀t≤150°C. Note *6 : Iso≤15.5A, dV/dt≤15V/ns, Vos peak≤600V, T₀t≤150°C.

Electrical Characteristics at Tc=25°C (unless otherwise specified) Static Ratings

Parameter	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I₀=250µA		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I₀=250µA		2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	Ioss	V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	μA
		V _{DS} =480V V _{GS} =0V	<i>T</i> _{ch} =125°C	-	-	250	
Gate-Source Leakage Current	Igss	V _{DS} =0V V _{GS} =±30V		-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V I _D =7.8A		-	0.169	0.190	Ω
Gate resistance	RG	f=1MHz, open drain		-	10.9	-	Ω

Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g ts	V _{DS} =25V I _D =7.8A	7.2	14.5	-	S
Input Capacitance	Ciss	V _{DS} =400V	-	1130	-	
Output Capacitance	Coss	V _{GS} =0V	-	30	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	4.4	-	
Effective output capacitance, energy related (Note *7)	Co(er)	V _{DS} =0400V V _{GS} =0V	-	69	-	pF
Effective output capacitance, time related (Note *8)	Co(tr)	V₀s=0400V V₀s=0V I₀=constant	-	251	-	
	V_{DD} =400V, V_{GS} =10V	-	18	-		
Turn-On Time	tr	$I_{D}=7.8A,$	-	30	-	- ns
td(off)	t _{d(off)}	$R_{\rm G}$ =18Ω See Fig.3 and Fig.4	-	143	-	
Turn-Off Time	<i>t</i> r		-	22	-	
Total Gate Charge	QG		-	46	-	nC
Gate-Source Charge	QGS	V_{DD} =400V, V_{GS} =10V	-	12	-	
Gate-Drain Charge	QGD	_ /₀=15.5A _ See Fig.5	-	14	-	
Drain-Source crossover Charge	Qsw		-	7	-	

Note *7 : $C_{0(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V. Note *8 : $C_{0(er)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

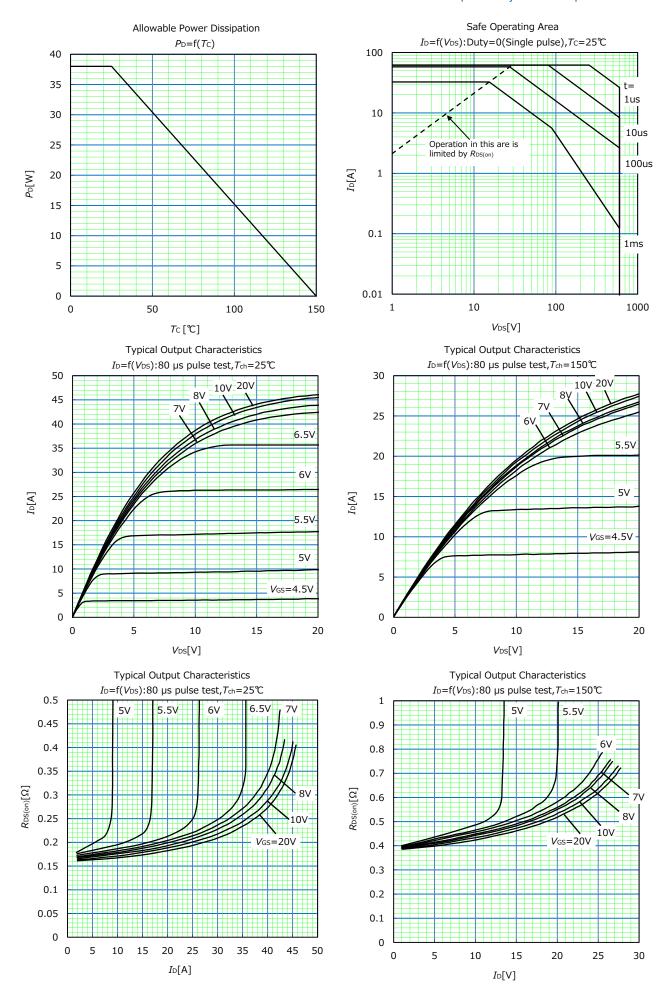
Reverse Diode

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode Forward On-Voltage	V _{SD}	I _{SD} =15.5A, V _{GS} =0V T _{ch} =25°C	-	0.90	1.35	V
Reverse Recovery Time	trr	- V _{op} =400V, / _{sp} =15.5A -di/dt=100A/μs 7 _{ch} =25°C See Fig.6 and Fig.7	-	328	-	ns
Reverse Recovery Charge	Qrr		-	4.2	-	μC
Peak Reverse Recovery Current	I _{rp}		-	25	-	А

Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)	-	-	3.29	°C/W
Channel to Ambient	Rth(ch-a)	-	-	58	°C/W

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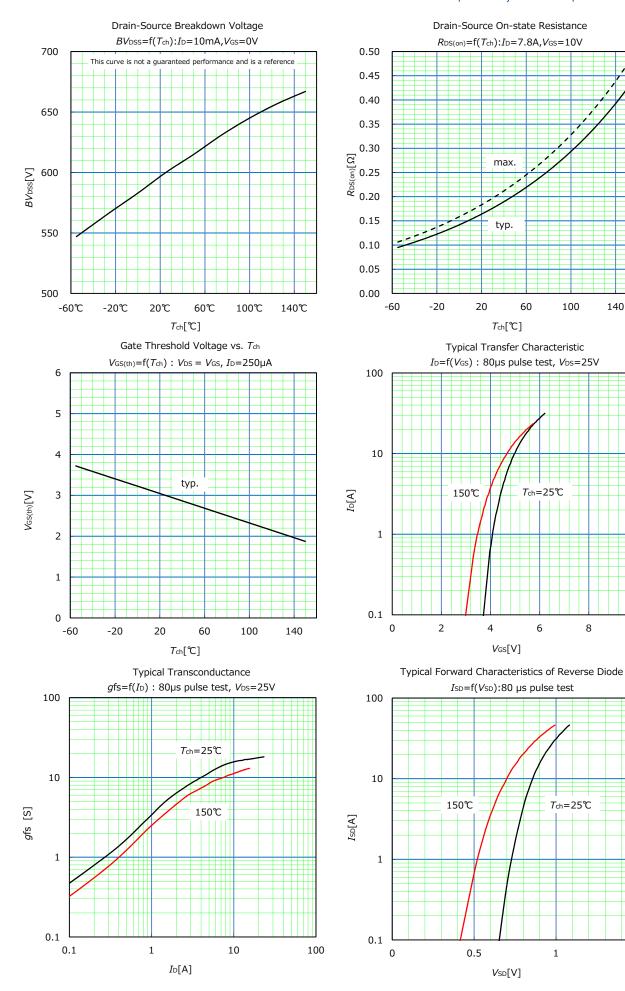


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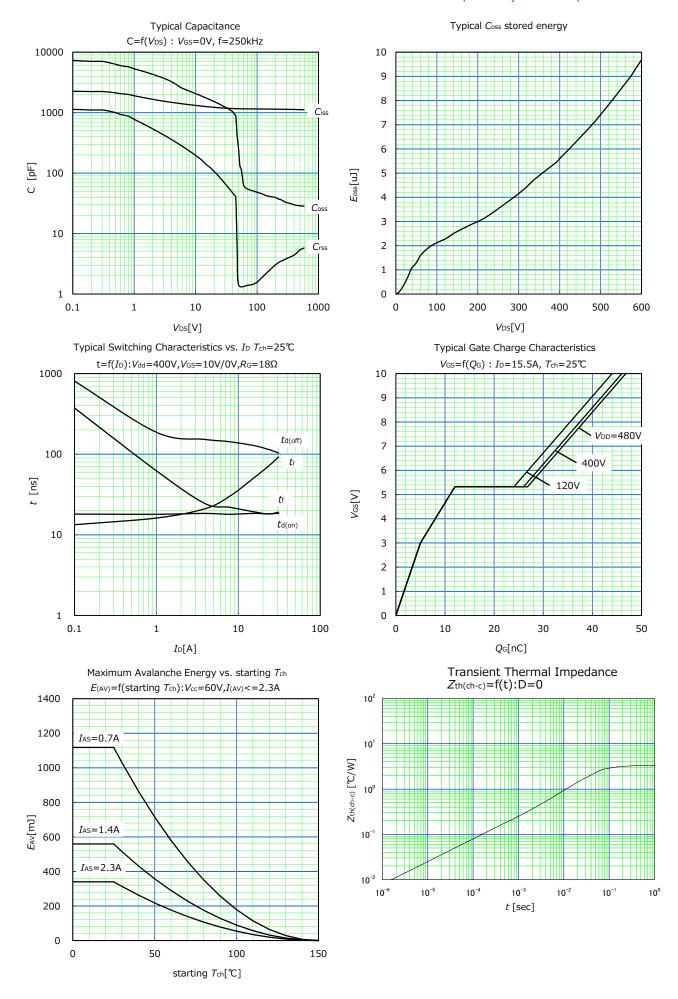
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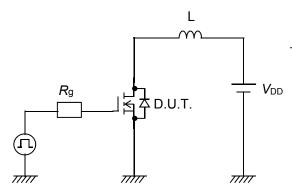
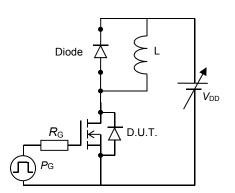


Fig.1 Avalanche Test circuit



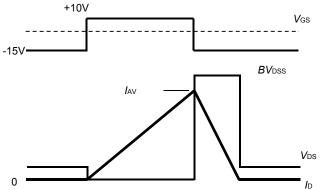


Fig.2 Operating waveforms of Avalanche Test

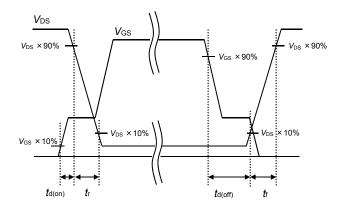


Fig.4 Operating waveform of Switching Test

Fig.3 Switching Test circuit

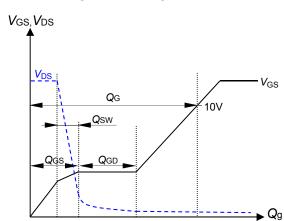
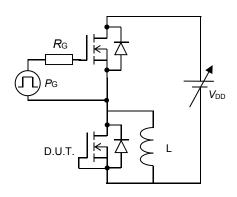


Fig.5 Operating waveform of Gate charge Test



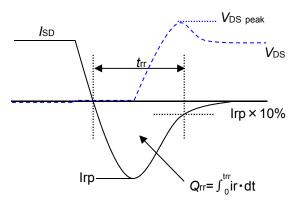


Fig.6 Reverse recovery Test circuit

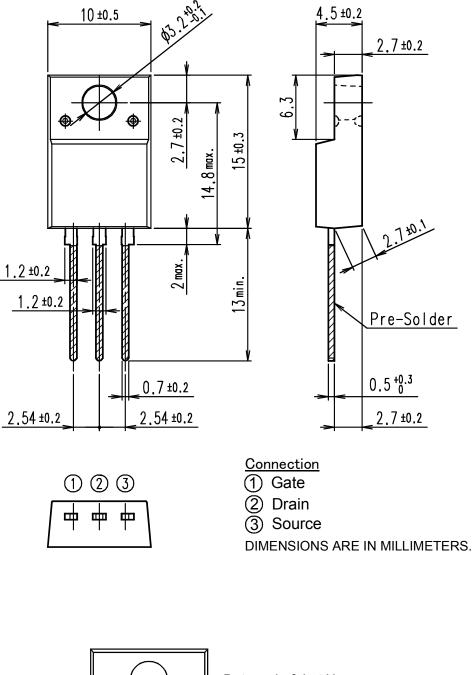
Fig.7 Operating waveform of Reverse recovery Test

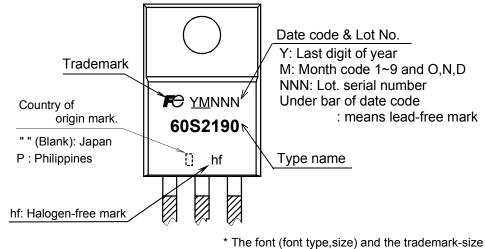
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Marking

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Outview: TO-220F(SLS) Package





I he font (font type,size) and the trademark-siz might be actually different.

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