- **S_o-Interface *MODULE:* *):**

Electrical specifications @ 25°C:

UMEC Part-No.**	Transformer									Choke				schematic
	n ±1%	ΔI_{dc} mA	L_H mH Min.	L_S uH Max.	C_K pF Max.	C_W PF Nom.	$R_{CU.IC}$ Ω Nom.	$R_{CU.L}$ Ω Nom.	U_P KVr ms	L_N mH	L_S µH Max.	R_{CU} Ω Nom.	U_P KVr ms	
Through hole:**														
UT21615	4:1/1	3	30	3	120	100	2.5	0.8	1.5	4x5	0.6	1.1	0.5	A
UT 28615	4:1/1	3	22	4	120	110	5.6	2.7	1.5	4x5	0.6	1.1	0.5	A
UT 28615A	4:1/1	3,6	30	3	120	145	2.5	1.2	1.5	4x5	0.6	1.1	0.5	A
UT21624	2/2:1/1	5	30	5	150	200	3.2	1.1	2.0	4x5	0.6	1.1	0.5	B
UT 28624	2/2:1/1	3.6	22	6	150	145	3.6	1.2	2.0	4.5	0.6	1.1	0.5	B
UT28624A	2/2:1/1	5	30	5	150	145	3.6	1.2	2.0	4.5	0.6	1.1	0.5	B
UT21626	2.5/2.5:1/1	5	30	5	150	250	6.0	1.6	1.5	4x5	0.6	1.1	0.5	B
SMT design:**														
UT21615-TS	4:1/1	3	30	3	120	100	2.5	0.8	1.5	4x5	0.6	1.1	0.5	A
UT21624-TS	2/2:1/1	5	30	5	150	200	3.2	1.1	2.0	4x5	0.6	1.1	0.5	B
UT28624A-T	2/2:1/1	5	30	5	150	145	3.6	1.2	2.0	4x5	0.6	1.1	0,5	B
UT21626-TS	2.5/2.5:1/1	5	30	5	150	250	6.0	1.6	2.0	4x5	0.6	1.1	0.5	B
EN60950-Design:														
UT 28615AN	4:1/1	3.6	30	3	120	150	4.6	1.4	3.0	4x5	0.6	1.05	0.5	A
UT21816	4:1:1	3.6	30	5	45	30	3.4	1.0	4.0	4x5	0.6	1.0	0.5	A

*) Pls.add suffix-TS ;Modules combine two So-tranformers and one current compensated 4-fold choke.

) Ferrite design solution **UT28xxx are available.

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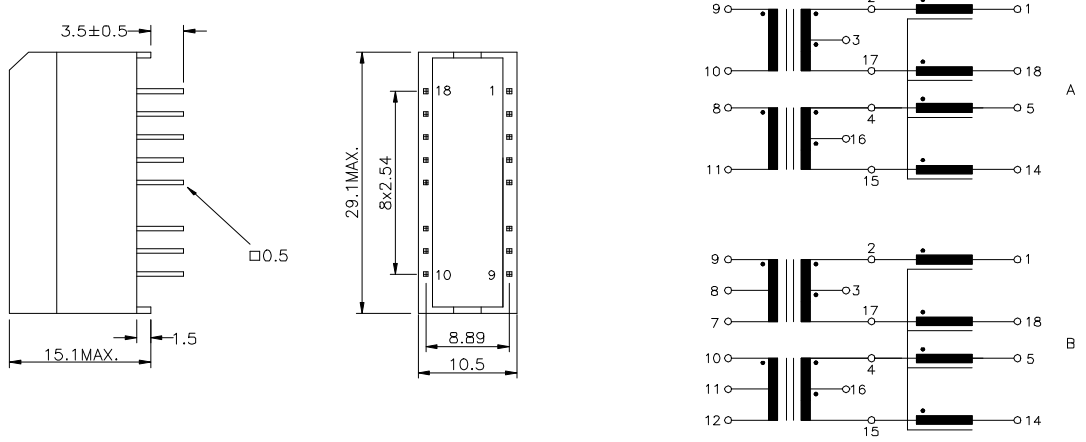
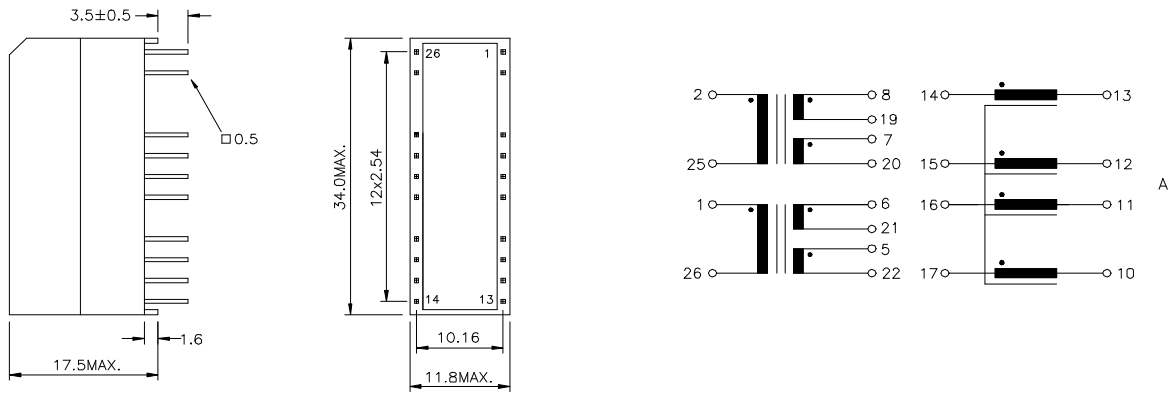
- **S_o-Interface *MODULE:* *):**

Dimensions and connections(tolerance=±0.2mm)

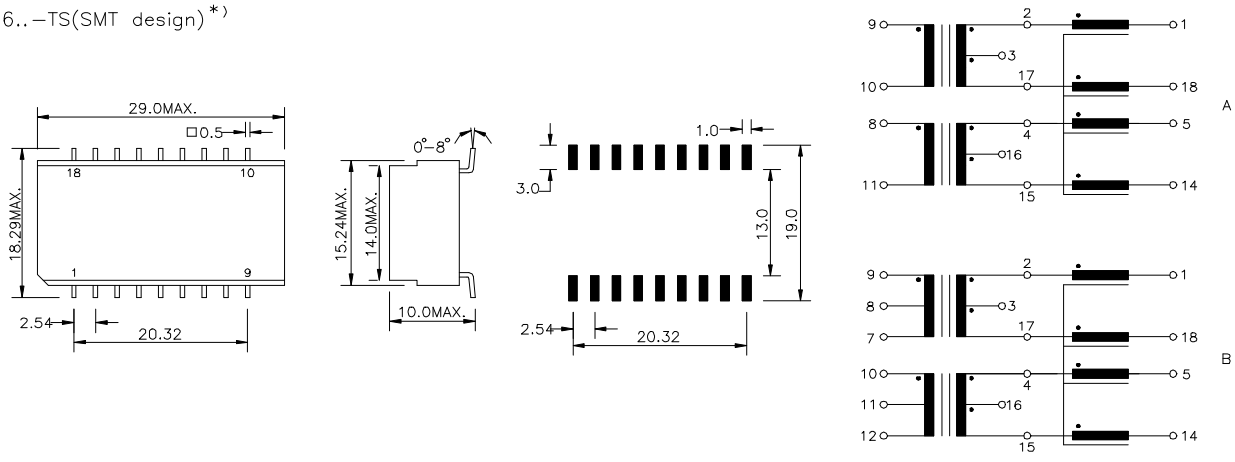
UT216..



UT218..



UT216..–TS(SMT design)*)



*)pins arrangement to customer requirement.

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TELECOMMUNICATIONS:

- **S_o-Interface *MODULE:* *):**

Definition of symbols:

Transformer:

n= transformer ratio: IC-side:Line-side.

ΔI_{dc}= max. permissible DC unbalance.

L_H= main inductance of winding(s) on Line-side(in series, f=10KHz U=100mVrms).

L_S= leakage inductance of winding(s) on Line-side with winding(s) on IC-side short circuited(each in series, f=100KHz U=100mVrms).

C_K= coupling capacitance between the winding(s) on IC-side and the winding(s) on Line-side(So-modules with each choke winding in series, f=10KHz U=100mVrms).

C_W= winding capacitance of winding(s) on Line-side(in series, nominal value, f=1MHz U=1Vrms).

$R_{CU.IC}$= DC resistance of the winding(s) on IC-side(in series, nominal value).

$R_{CU.L}$= DC resistance of the winding(s) on Line-side(in series, nominal value).

U_P= test voltage, rms value 50/60Hz, 2seconds, winding(s) on Line-side to winding(s) on IC-side.

Choke:

L_N= rated inductance of a winding(tol. +50%/-30%, f=10KHz U=100mVrms).

L_S= leakage inductance of winding when all other windings short circuited(nominal value, f=100KHz U=100mVrms).

R_{CU}= DC resistance of each winding(nominal value).

U_P=test voltage, rms value 50/60Hz, 2seconds, winding to winding.

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