

MJE13003

SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- Reverse Biased SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 A, 25 and 100°C
 t_c @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C I_{CM}	1.5 3	Adc
Base Current – Continuous – Peak (Note 1)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current – Continuous – Peak (Note 1)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.4 11.2	W mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 320	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.12	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	89	$^\circ\text{C}/\text{W}$
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

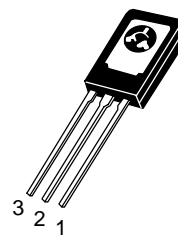
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

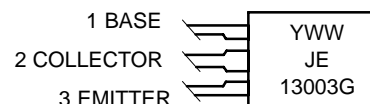
<http://onsemi.com>

**1.5 AMPERES
NPN SILICON POWER
TRANSISTORS
300 AND 400 VOLTS
40 WATTS**



TO-225
CASE 77
STYLE 3

MARKING DIAGRAM



Y = Year
WW = Work Week
JE13003 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO-225	500 Units/Box
MJE13003G	TO-225 (Pb-Free)	500 Units/Box

MJE13003

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (Note 2)

Collector–Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	–	–	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with bass forward biased	$I_{S/b}$	See Figure 11			–
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			–

ON CHARACTERISTICS (Note 2)

DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 1\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	8 5	– –	40 25	–
Collector–Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	– – – –	– – – –	0.5 1 3 1	Vdc
Base–Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	– – –	– – –	1 1.2 1.1	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ($I_C = 100\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	10	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	–	21	–	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 125\text{ Vdc}$, $I_C = 1\text{ A}$, $I_{B1} = I_{B2} = 0.2\text{ A}$, $t_p = 25\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$)	t_d	–	0.05	0.1	μs
Rise Time		t_r	–	0.5	1	μs
Storage Time		t_s	–	2	4	μs
Fall Time		t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	$(I_C = 1\text{ A}$, $V_{clamp} = 300\text{ Vdc}$, $I_{B1} = 0.2\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	–	1.7	4	μs
Crossover Time		t_c	–	0.29	0.75	μs
Fall Time		t_{fi}	–	0.15	–	μs

2. Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

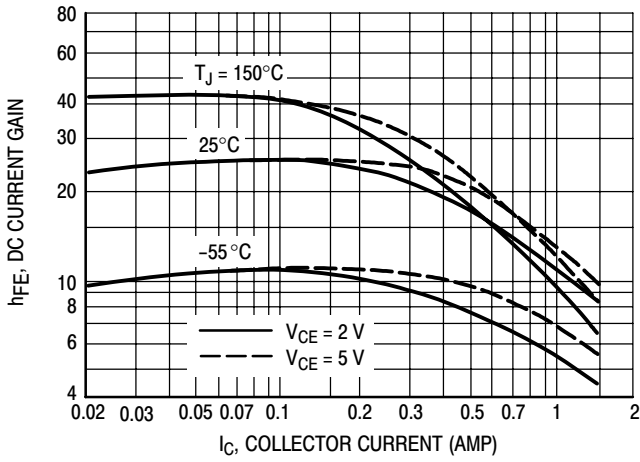


Figure 1. DC Current Gain

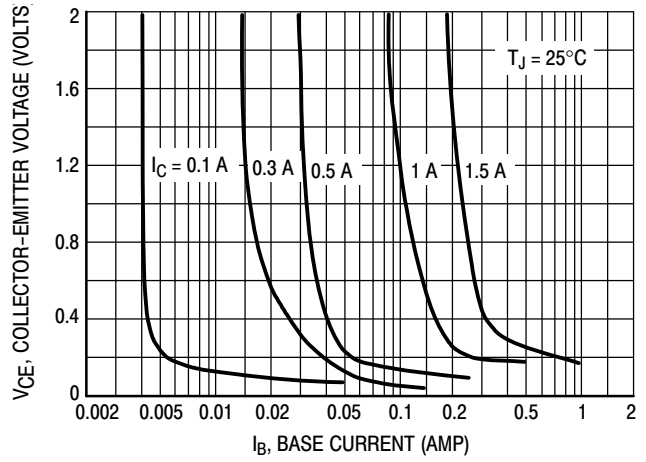


Figure 2. Collector Saturation Region

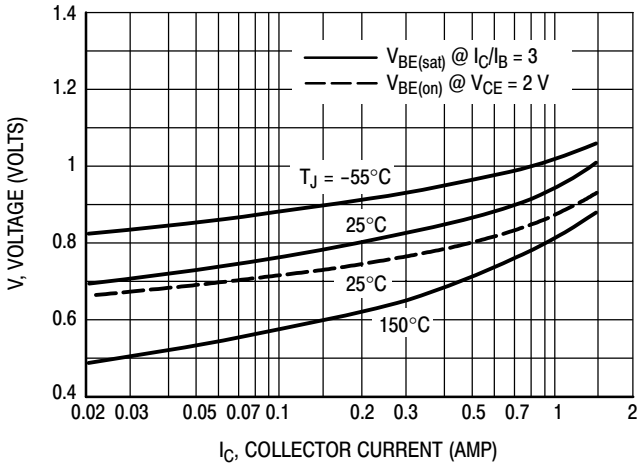


Figure 3. Base-Emitter Voltage

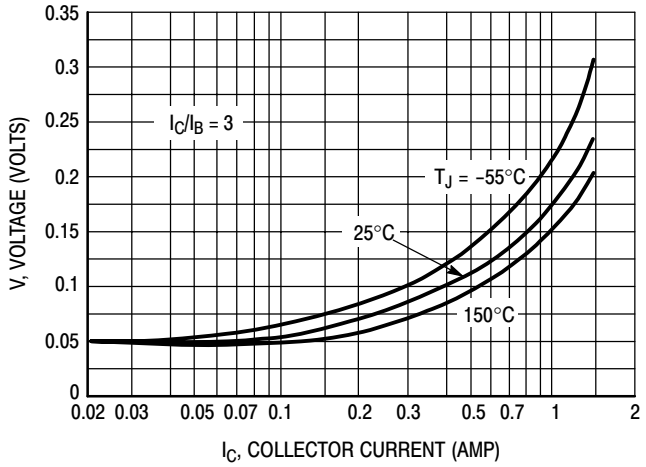


Figure 4. Collector-Emitter Saturation Region

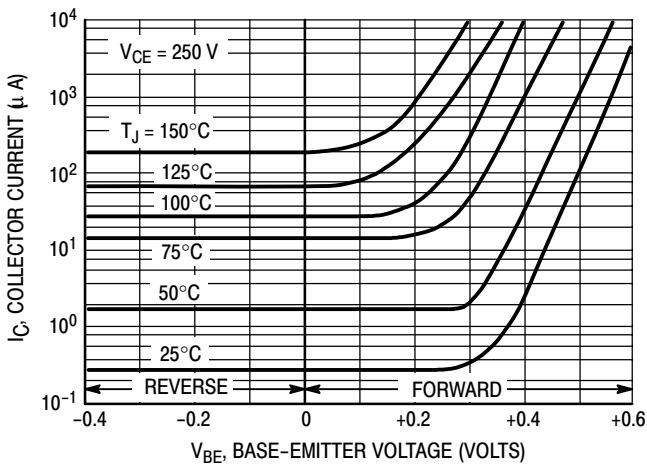


Figure 5. Collector Cutoff Region

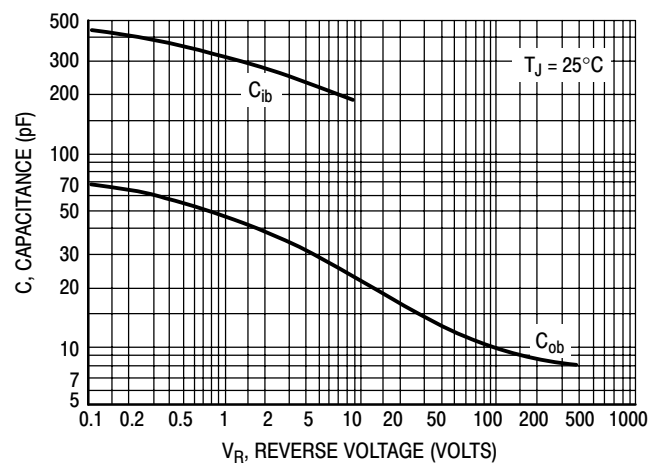


Figure 6. Capacitance

MJE13003

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
TEST CIRCUITS	<p>DUTY CYCLE $\leq 10\%$ $t_r, t_f \leq 10 \text{ ns}$</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	<p>*SELECTED FOR $\geq 1 \text{ kV}$</p>	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2 A $L_{\text{coil}} = 50 \text{ mH}$	$V_{CC} = 20 \text{ V}$ $V_{\text{clamp}} = 300 \text{ Vdc}$	$V_{CC} = 125 \text{ V}$ $R_C = 125 \Omega$ $D1 = 1\text{N}5820 \text{ or Equiv.}$ $R_B = 47 \Omega$
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{\text{coil}} (I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}} (I_{C_{pk}})}{V_{\text{clamp}}}$ <p>Test Equipment Scope—Tektronics 475 or Equivalent</p>	<p>$t_r, t_f < 10 \text{ ns}$ Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>	

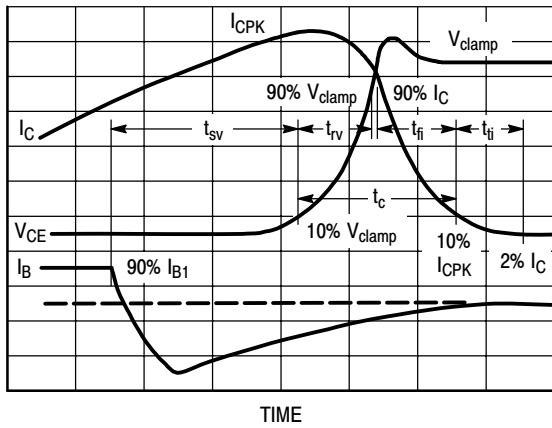


Figure 7. Inductive Switching Measurements

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μS	t_{rv} μS	t_{fi} μS	t_{ti} μS	t_c μS
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC}I_C(t_c)f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

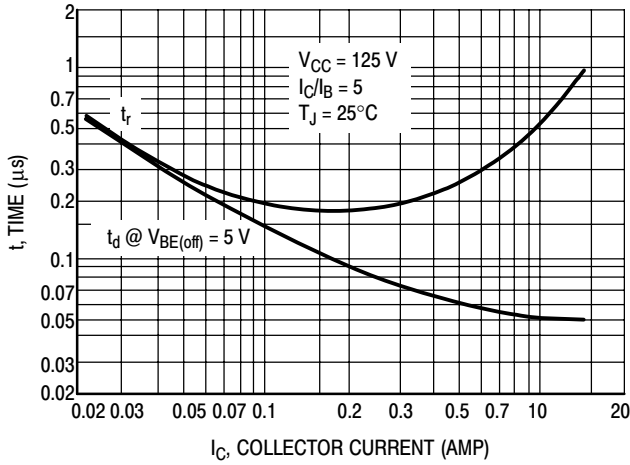


Figure 8. Turn-On Time

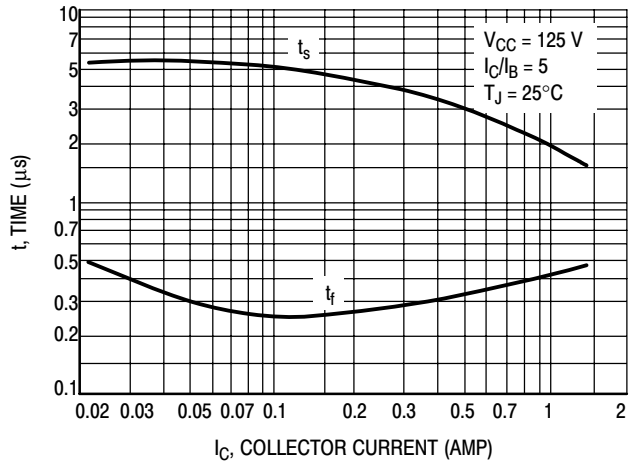


Figure 9. Turn-Off Time

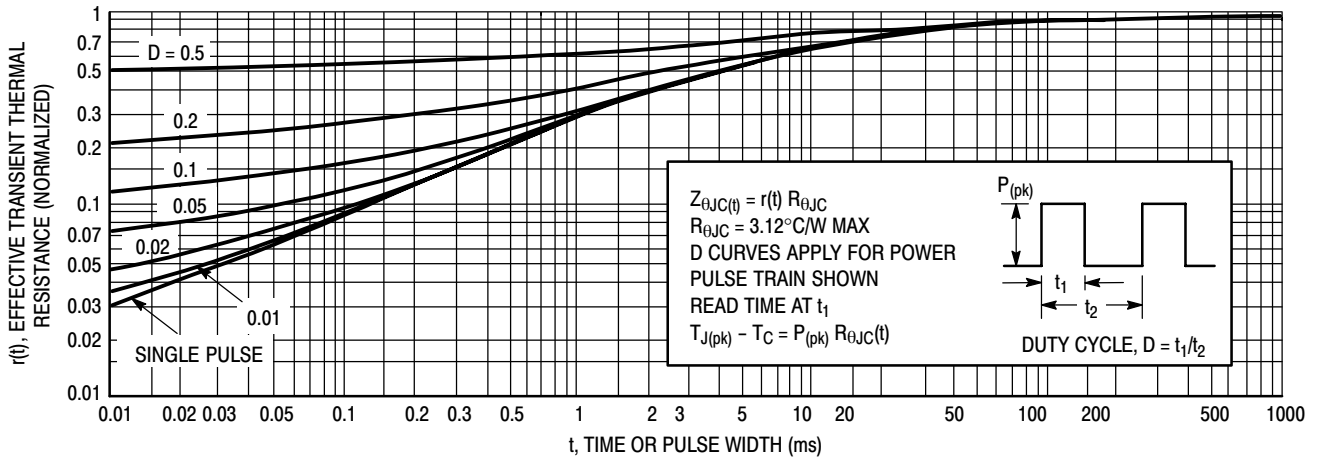


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

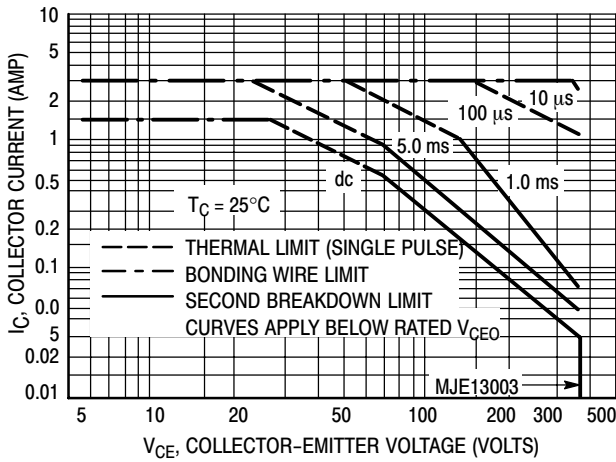


Figure 11. Active Region Safe Operating Area

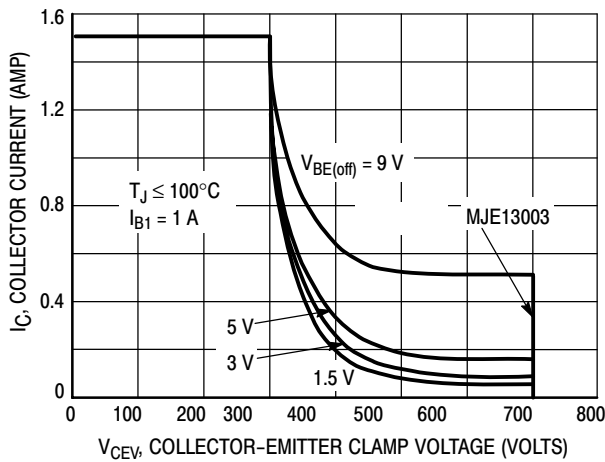


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

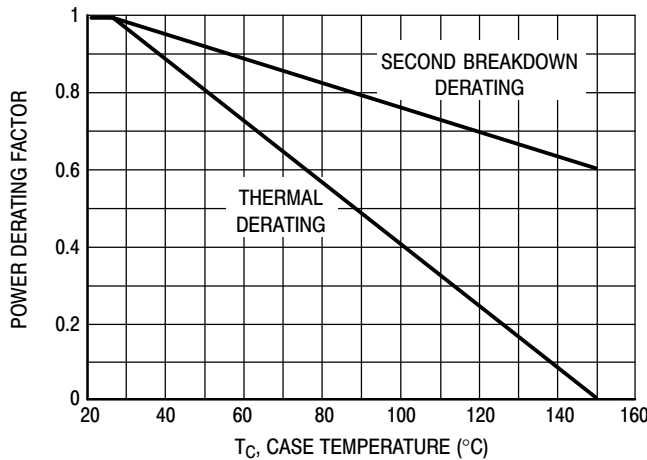
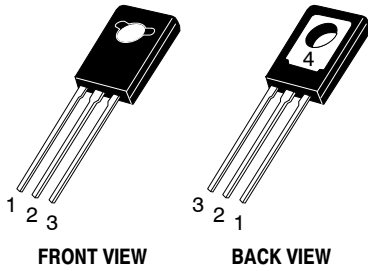


Figure 13. Forward Bias Power Derating

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

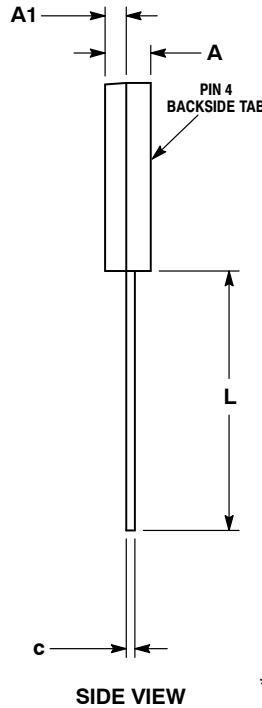
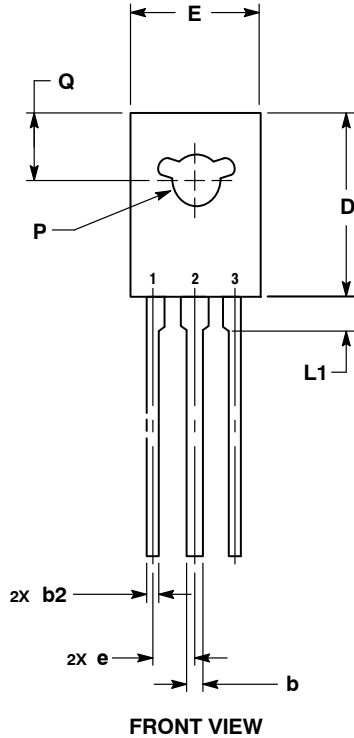
ON Semiconductor®



TO-225
CASE 77-09
ISSUE AD

DATE 25 MAR 2015

SCALE 1:1

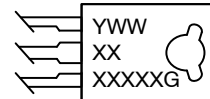


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



- Y = Year
- WW = Work Week
- XXXXX = Device Code
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present.

- | | | | | |
|---|---|---|---|---|
| <p>STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE</p> | <p>STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE</p> | <p>STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER</p> | <p>STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE</p> | <p>STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE</p> |
| <p>STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE</p> | <p>STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2</p> | <p>STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN</p> | <p>STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE</p> | <p>STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE</p> |

DOCUMENT NUMBER:	98ASB42049B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-225	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[MJE13003](#) [MJE13003G](#)