N-Channel Power MOSFET

650V, 2.0A, 5Ω

FEATURES

- 100% UIS & R_g tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

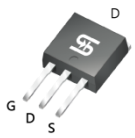
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	650	V
$R_{DS(on)}$ (max)	5	Ω
Q_g	13	nC

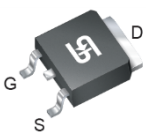
APPLICATION

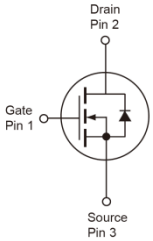
- Power Supply
- AC/DC LED Lighting

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-251 (IPAK SL) **TO-252 (DPAK)**







Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	2.0	A
	T_C = 100°C		1.4	
Pulsed Drain Current (Note 1)		I_{DM}	8.0	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	65	W
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	25	mJ
Single Pulsed Avalanche Current (Note 2)		I_{AS}	1.6	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.9	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62.5	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	650	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2	2.5	4	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	I_{DSS}	--	--	10	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 1A	$R_{DS(ON)}$	--	4	5	Ω
Forward Transfer Conductance	V_{DS} = 10V, I_D = 1A	g_{fs}	--	2.5	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = 520V, I_D = 2A, V_{GS} = 10V	Q_g	--	13	--	nC
Gate-Source Charge		Q_{gs}	--	2.2	--	
Gate-Drain Charge		Q_{gd}	--	5	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, F = 1.0MHz	C_{iss}	--	390	--	pF
Output Capacitance		C_{oss}	--	31	--	
Reverse Transfer Capacitance		C_{rss}	--	8	--	
Gate Resistance	f = 1.0MHz, open drain	R_g	0.8	2.5	7.5	Ω
Switching (Note 5)						
Turn-On Delay Time	V_{GS} = 10V, I_D = 2A, V_{DD} = 325V, R_G =25Ω	$t_{d(on)}$	--	8.2	--	ns
Turn-On Rise Time		t_r	--	23.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	38	--	
Turn-Off Fall Time		t_f	--	27	--	
Source-Drain Diode (Note 3)						
Diode Forward Voltage	I_S = 2A, V_{GS} = 0V	V_{SD}	--	--	1.2	V

Notes:

1. Pulse width limited by the maximum junction temperature
2. L = 20mH, I_{AS} = 1.6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
4. For DESIGN AID ONLY, not subject to production testing.
5. Essentially Independent of Operating Temperature.

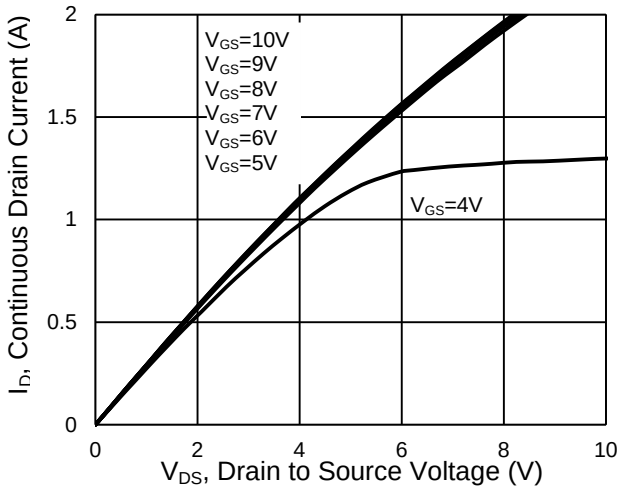
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2NB65CH X0G	TO-251S	75pcs / Tube
TSM2NB65CP ROG	TO-252	2,500pcs / 13” Reel

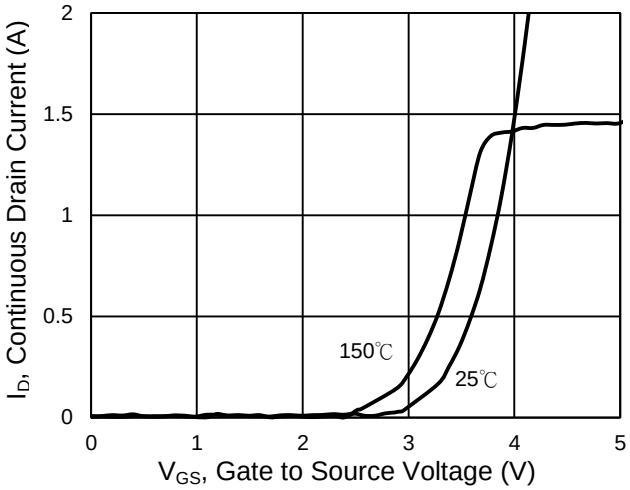
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

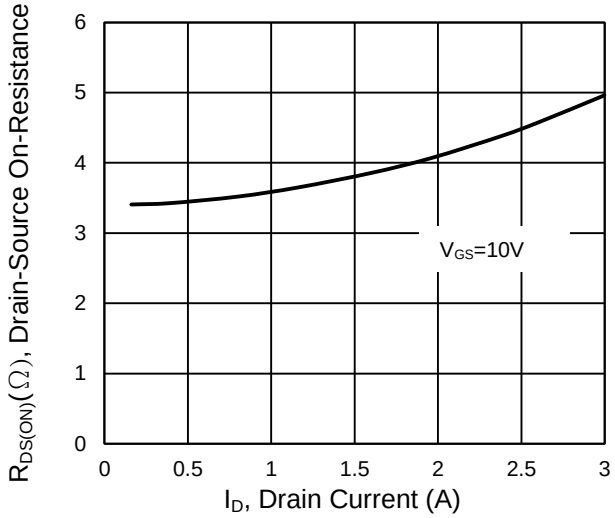
Output Characteristics



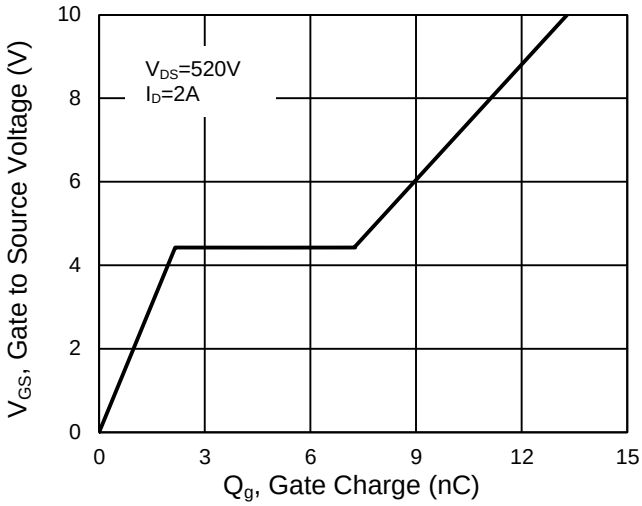
Transfer Characteristics



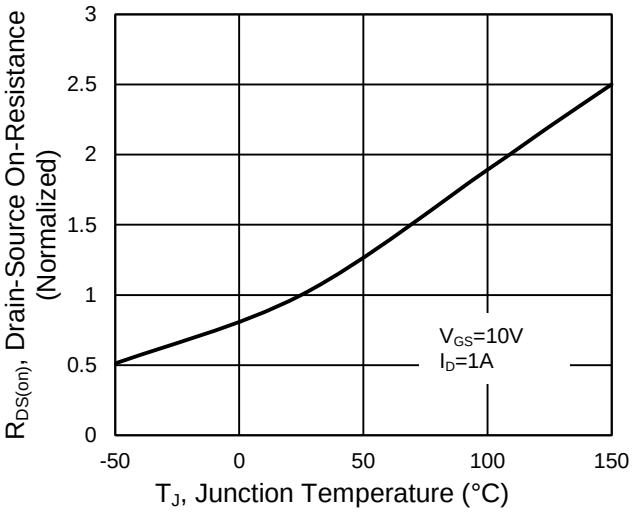
On-Resistance vs. Drain Current



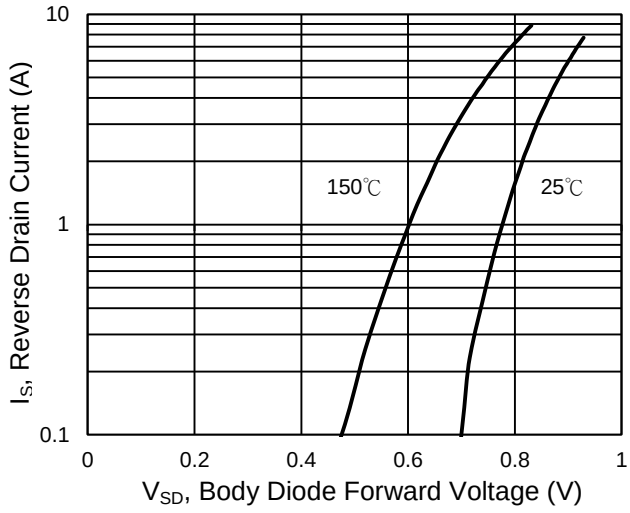
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



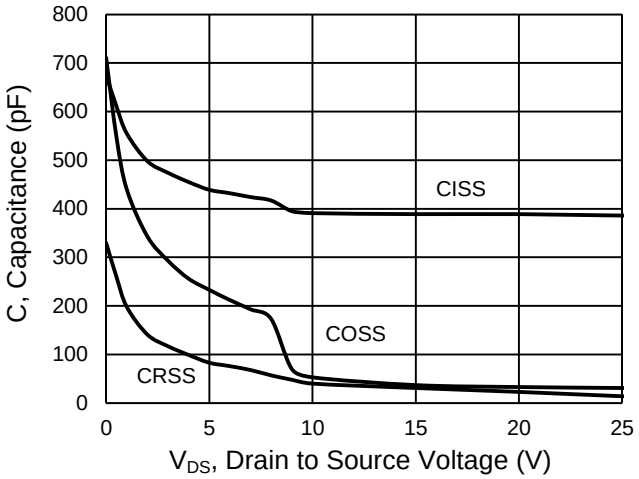
Source-Drain Diode Forward Current vs. Voltage



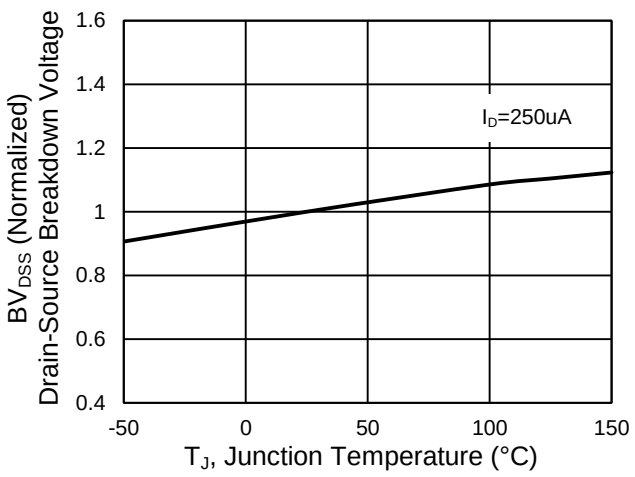
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

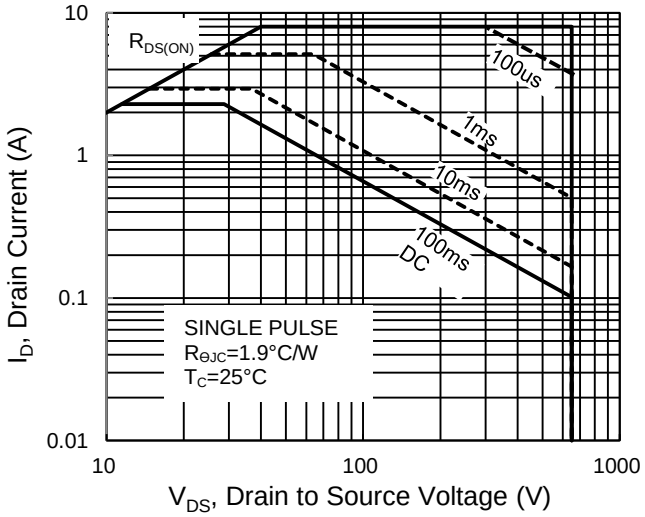
Capacitance vs. Drain-Source Voltage



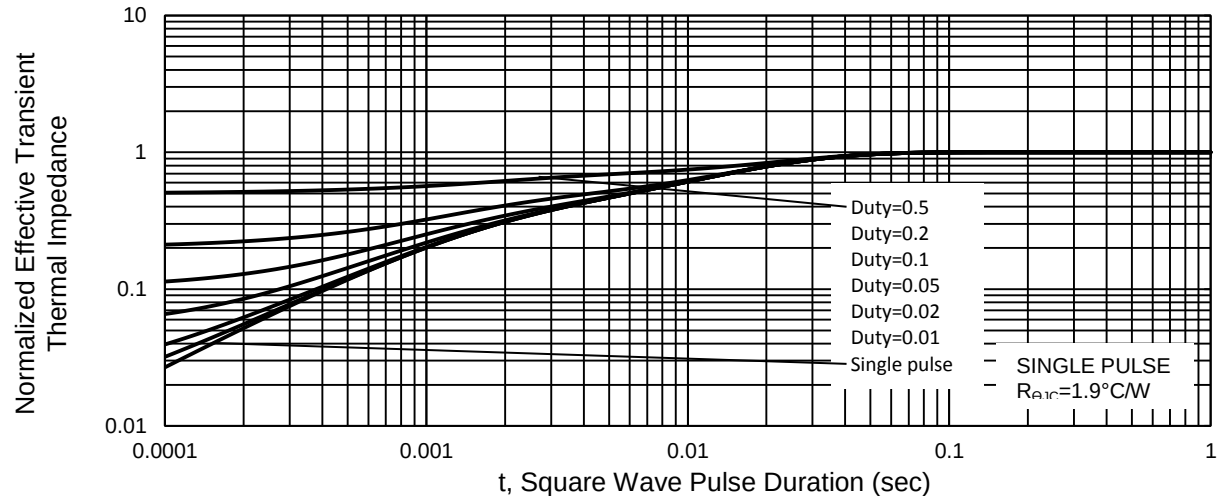
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area (TO-251/252)

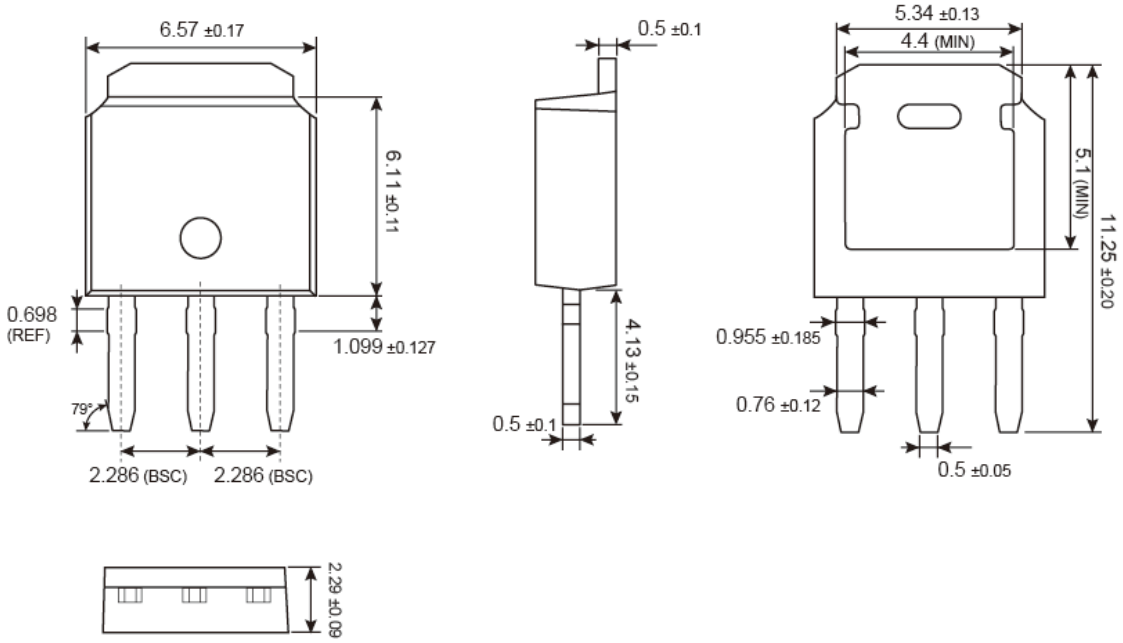


Normalized Thermal Transient Impedance, Junction-to-Case (TO-251/252)

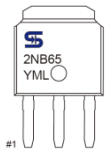


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251S



MARKING DIAGRAM



Y = Year Code

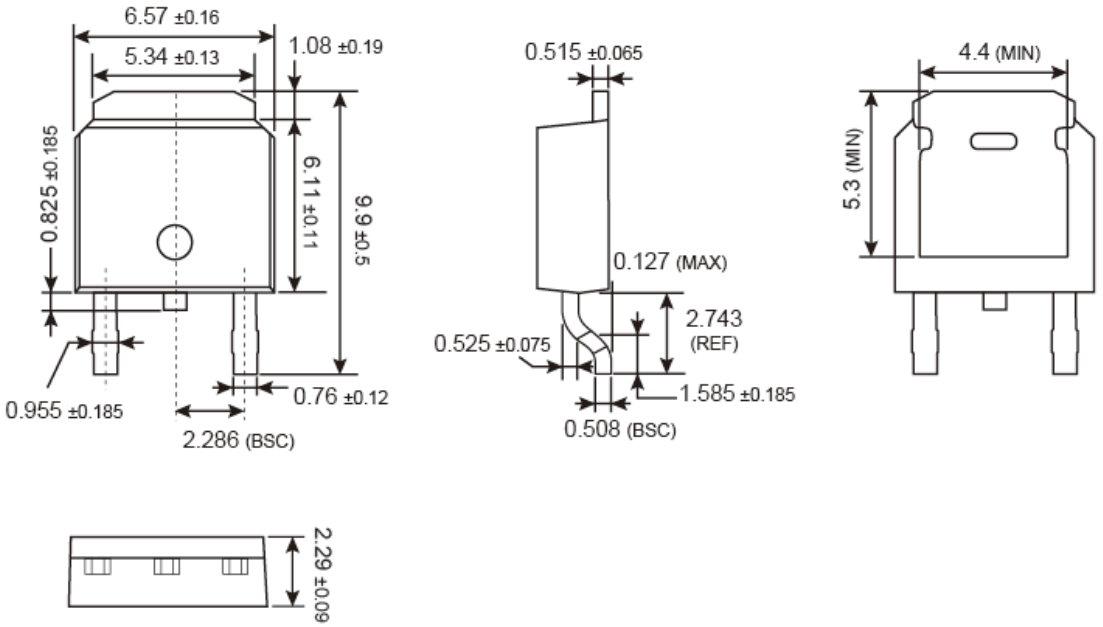
M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

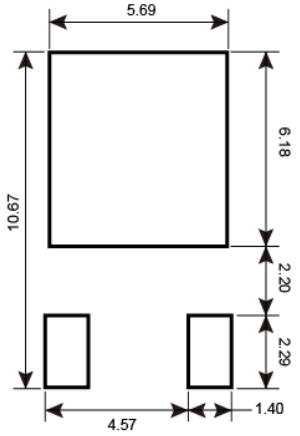
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

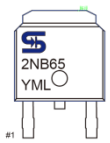
TO-252



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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