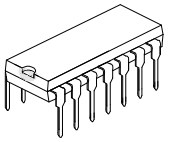
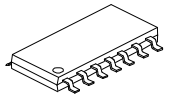
# CD4541

*CMOS IC*

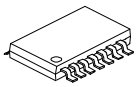
## PROGRAMMABLE TIMER



DIP-14



SOP-14



TSSOP-14

### ■ DESCRIPTION

The **CD4541** programmable timer comprise a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

### ■ FEATURES

* Operates at $2^n$ frequency divider or as single transition timer
* Increments on positive edge clock transitions
* Wide supply voltage range: 3.0V ~ 15V
* Built-in low power RC oscillator
* Oscillator frequency range ~ DC to 100 kHz
* External clock applied to Pin 3 can be used instead of oscillator
* Available division ratios $2^8$, $2^{10}$, $2^{13}$, or $2^{16}$
* High noise immunity: 0.45 $V_{DD}$ (typ)
* Master reset totally independent of automatic reset operation
* Automatic reset initializes all counters when power turns on
* Q/$\overline{Q}$ select provides output logic level flexibility
* High output drive min. one TTL load
* Maximum input leakage 1μA at 15V over full temperature range

### ■ ORDERING INFORMATION

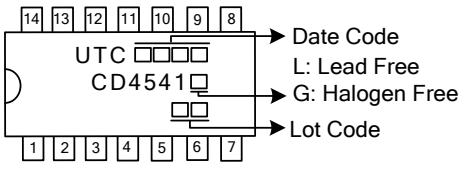
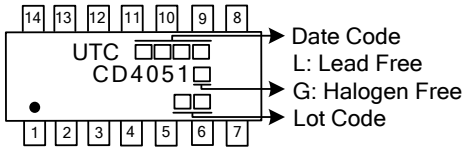
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| CD4541L-D14-T | CD4541G-D14-T | DIP-14 | Tube |
| CD4541L-S14-R | CD4541G-S14-R | SOP-14 | Tape Reel |
| CD4541L-P14-R | CD4541G-P14-R | TSSOP-14 | Tape Reel |

CD4541G-D14-T

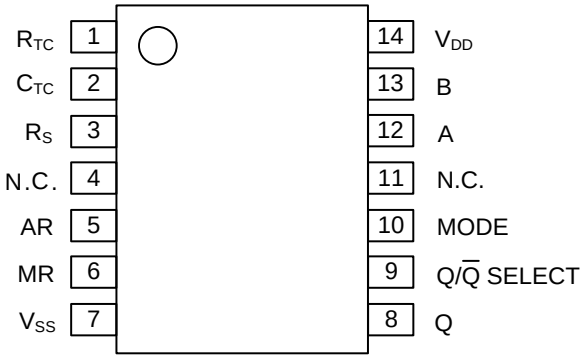
(1)Packing Type
(2)Package Type
(3)Green Package

(1) T: Tube, R: Tape Reel
(2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

### ■ MARKING

| DIP-14 | SOP-14 / TSSOP-14 |
|---|---|
|  |  |

## ■ PIN CONFIGURATION



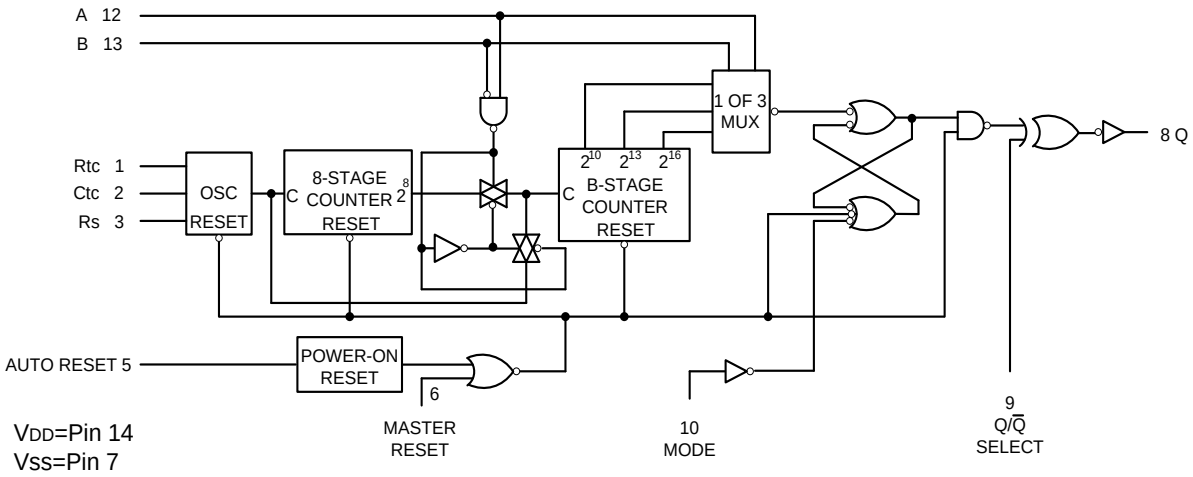

## ■ TRUTH TABLE

| PIN | STATE | |
|---|---|---|
| | 0 | 1 |
| 5 | Auto Reset Operating | Auto Reset Disabled |
| 6 | Timer Operational | Master Reset On |
| 9 | Output Initially Low after Reset | Output Initially High after Reset |
| 10 | Single Cycle Mode | Recycle Mode |

## ■ DIVISION RATIO TABLE

| A | B | Number of Counter Stages<br>n | Count<br>$2^n$ |
|---|---|---|---|
| 0 | 0 | 13 | 8192 |
| 0 | 1 | 10 | 1024 |
| 1 | 0 | 8 | 256 |
| 1 | 1 | 16 | 65536 |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | -0.5 ~ +18 | V |
| Input Voltage | | $V_{IN}$ | -0.5 ~ $V_{DD}$+0.5 | V |
| Power Dissipation | DIP-14 | $P_D$ | 700 | mW |
| | SOP-14<br>TSSOP-14 | | 500 | |
| Junction Temperature | | $T_J$ | 125 | °C |
| Operating Temperature | | $T_{OPR}$ | -20 ~ +85 | °C |
| Storage Temperature | | $T_{STG}$ | -40 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3 ~ 15 | V |
| Input Voltage | $V_{IN}$ | 0 ~ $V_{DD}$ | V |
| Operating Temperature | $T_{OPR}$ | -40 ~ +85 | °C |

## ■ DC ELECTRICAL CHARACTERISTICS ($T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Quiescent Device Current | $I_{DD}$ | $V_{DD}$= 5V, $V_{IN}$=$V_{DD}$ or $V_{SS}$ | | 0.005 | 20 | μA |
| | | $V_{DD}$=10V, $V_{IN}$=$V_{DD}$ or $V_{SS}$ | | 0.010 | 40 | |
| | | $V_{DD}$=15V, $V_{IN}$=$V_{DD}$ or $V_{SS}$ | | 0.015 | 80 | |
| Low Level Output Voltage | $V_{OL}$ | $V_{DD}$=5V | | 0 | 0.05 | V |
| | | $V_{DD}$=10V, I $I_O$ I<1μA | | 0 | 0.05 | |
| | | $V_{DD}$=15V | | 0 | 0.05 | |
| High Level Output Voltage | $V_{OH}$ | $V_{DD}$=5V | 4.95 | 5 | | V |
| | | $V_{DD}$=10V, I $I_O$ I<1μA | 9.95 | 10 | | |
| | | $V_{DD}$=15V | 14.95 | 15 | | |
| Low Level Input Voltage | $V_{IL}$ | $V_{DD}$=5V, $V_O$=0.5V or 4.5V | | 2 | 1.5 | V |
| | | $V_{DD}$=10V, $V_O$=1.0V or 9.0V | | 4 | 3.0 | |
| | | $V_{DD}$=15V, $V_O$=1.5V or 13.5V | | 6 | 4.0 | |
| High Level Input Voltage | $V_{IH}$ | $V_{DD}$=5V, $V_O$=0.5V or 4.5V | 3.5 | 3 | | V |
| | | $V_{DD}$=10V, $V_O$=1.0V or 9.0V | 7.0 | 6 | | |
| | | $V_{DD}$=15V, $V_O$=1.5V or 13.5V | 11.0 | 9 | | |
| Low Level Output Current (Note) | $I_{OL}$ | $V_{DD}$=5V, $V_O$=0.4V | 1.96 | 3.6 | | mA |
| | | $V_{DD}$=10V, $V_O$=0.5V | 2.66 | 9.0 | | |
| | | $V_{DD}$=15V, $V_O$=1.5V | 10.4 | 34.0 | | |
| High Level Output Current (Note) | $I_{OH}$ | $V_{DD}$=5V, $V_O$=2.5V | 4.27 | 130 | | mA |
| | | $V_{DD}$=10V, $V_O$=9.5V | 2.25 | 8.0 | | |
| | | $V_{DD}$=15V, $V_O$=13.5V | 8.8 | 30.0 | | |
| Input Current | $I_{IN}$ | $V_{DD}$=15V, $V_{IN}$=0V | | $-10^{-5}$ | -0.3 | μA |
| | | $V_{DD}$=15V, $V_{IN}$=15V | | $10^{-5}$ | 0.3 | |

Note: $I_{OH}$ and $I_{OL}$ are tested one output at a time.

## ■ AC ELECTRICAL CHARACTERISTICS (Note 1, $T_A$=25°C, $C_L$=50pF (refer to test circuits))

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | $V_{DD}$=5V | | 50 | 200 | ns |
| | | $V_{DD}$=10V | | 30 | 100 | |
| | | $V_{DD}$=15V | | 25 | 80 | |
| Output Fall Time | $t_{THL}$ | $V_{DD}$=5V | | 50 | 200 | ns |
| | | $V_{DD}$=10V | | 30 | 100 | |
| | | $V_{DD}$=15V | | 25 | 80 | |
| Turn-Off, Turn-On Propagation Delay, Clock to Q ($2^8$ Output) | $t_{PLH}$, $t_{PHL}$ | $V_{DD}$=5V | | 1.8 | 4.0 | μs |
| | | $V_{DD}$=10V | | 0.6 | 1.5 | |
| | | $V_{DD}$=15V | | 0.4 | 1.0 | |
| Turn-On, Turn-Off Propagation Delay, Clock to Q ($2^{16}$ Output) | $t_{PHL}$, $t_{PLH}$ | $V_{DD}$=5V | | 3.2 | 8.0 | μs |
| | | $V_{DD}$=10V | | 1.5 | 3.0 | |
| | | $V_{DD}$=15V | | 1.0 | 2.0 | |
| Clock Pulse Width | $t_{WH(CL)}$ | $V_{DD}$=5V | 400 | 200 | | ns |
| | | $V_{DD}$=10V | 200 | 100 | | |
| | | $V_{DD}$=15V | 150 | 70 | | |
| Clock Pulse Frequency | $f_{CL}$ | $V_{DD}$=5V | | 2.5 | 1.0 | MHz |
| | | $V_{DD}$=10V | | 6.0 | 3.0 | |
| | | $V_{DD}$=15V | | 8.5 | 4.0 | |
| MR Pulse Width | $t_{WH(R)}$ | $V_{DD}$=5V | 400 | 170 | | ns |
| | | $V_{DD}$=10V | 200 | 75 | | |
| | | $V_{DD}$=15V | 150 | 50 | | |
| Average Input Capacitance | $C_I$ | Any Input | | 5.0 | 7.5 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | (Note 2) | | 100 | | pF |

Notes: 1. AC Parameters are guaranteed by DC correlated testing.
2. $C_{PD}$ determines the no load AC power consumption of any CMOS device.

## ■ OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f=\frac{1}{2.3\ R_{TC}C_{TC}} \text{ if } (1\ kHz \leqq f \leqq 100kHz)$$

and RS ~ 2 $R_{TC}$ where RS≧10 kΩ

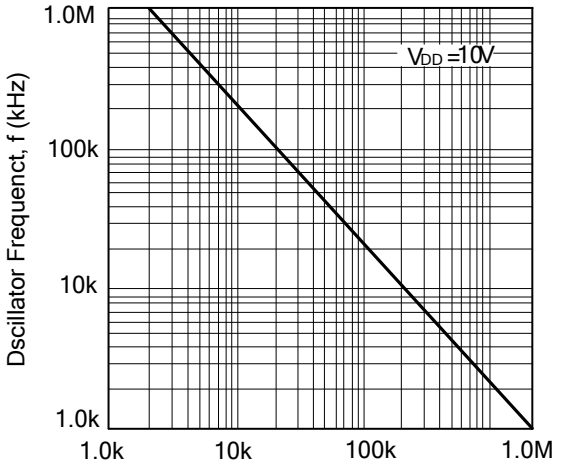
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages ($2^8$, $2^{10}$, $2^{13}$, and $2^{16}$). The $2^n$ counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is “1”, $2^{16}$ is selected for both states of B.

However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting $2^8$).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/Q select pin is set to a “0” the Q output is a “0”. Correspondingly, when Q/$\overline{Q}$ select pin is set to a “1” the Q output is a “1”.

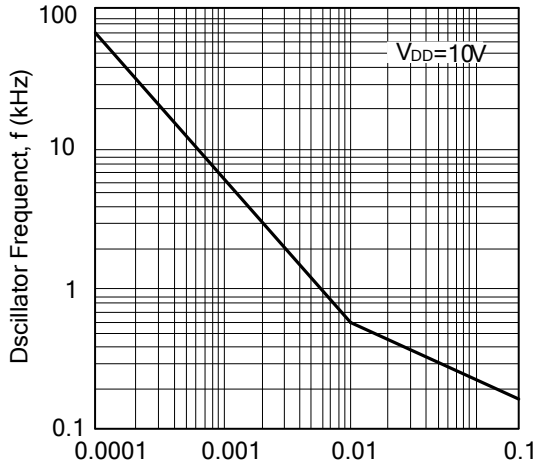
When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after $2^{n-1}$ counts the RS flip-flop sets which causes the output to change state. Hence, after another $2^{n-1}$ counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

RC Oscillator Frequency as a Function of $R_{TC}$ and C



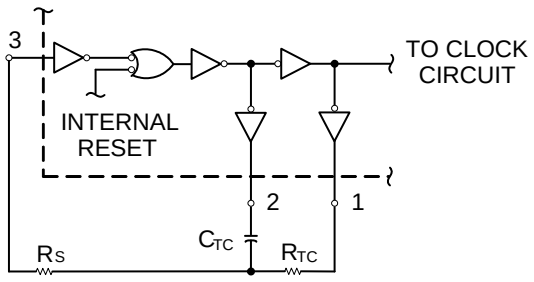

f as a function of $R_{TC}$ and (C=100pF, Rs=2$R_{TC}$)

RC Oscillator Frequency as a Function of $R_{TC}$ and C



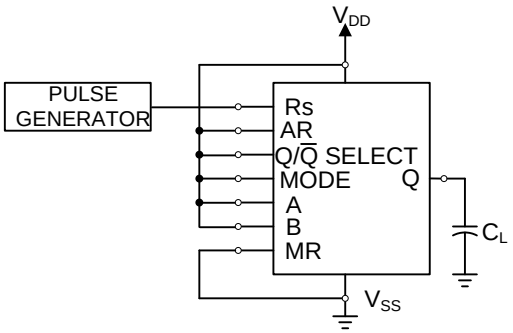

f as a function of C and ($R_{TC}$=56KΩ,Rs=120k)

Oscillator Circuit Using RC Configuration

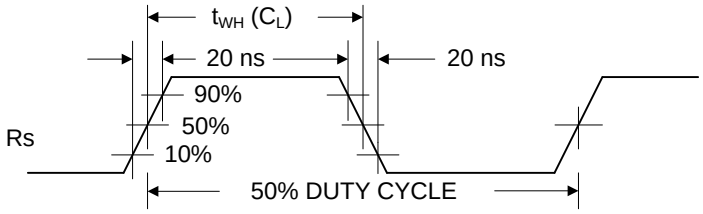


## ■ TEST CIRCUIT AND WAVEFORMS

Power Dissipation Test Circuit and Waveforms




(Rtc and Ctc outputs are left open)




Switching Time Test Circuit and Waveforms