
**I²C-Compatible (2-wire) Serial EEPROM
512-Kbit (65,536 x 8)**

DATASHEET

Features

- Low-voltage and Standard-voltage Operation
 - $V_{CC} = 1.7V$ to $3.6V$
 - $V_{CC} = 2.5V$ to $5.5V$
- Internally Organized as 65,536 x 8 (512K)
- I²C-Compatible (2-Wire) Serial Interface
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz (1.7V) and 1MHz (2.5V, 5.5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 128-byte Page Write Mode
 - Partial Page Writes Allowed
- Random and Sequential Read Modes
- Self-timed Write Cycle (5ms Max)
- High Reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 40 Years
- Green Package Options (Pb/Halide-free/RoHS Compliant)
 - 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, 8-pad UDFN, 8-ball WLCSP, and 8-ball VFBGA Packages
- Die sale Options: Wafer Form and Tape and Reel Available

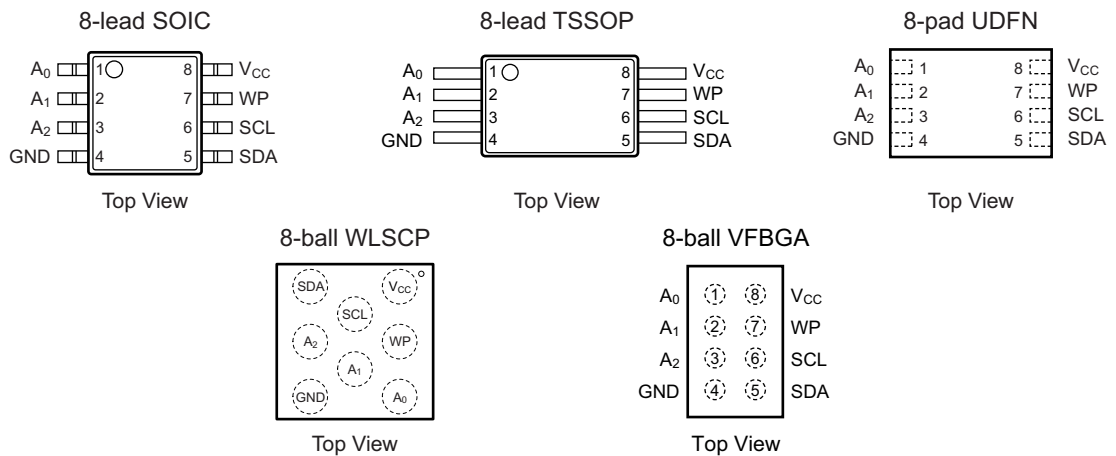
Description

The Atmel® AT24C512C provides 524,288 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 65,536 words of 8 bits each. The cascadable feature of the device allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, 8-pad UDFN, 8-ball WLCSP, and 8-ball VFBGA packages. In addition, the entire family is available in 1.7V to 3.6V and 2.5V to 5.5V versions.

1. Pin Configurations and Pinouts

Figure 1. Pin Configurations

| Pin Name | Function |
|--|--------------------|
| A ₀ , A ₁ , A ₂ | Address Inputs |
| GND | Ground |
| SDA | Serial Data |
| SCL | Serial Clock Input |
| WP | Write Protect |
| V _{CC} | Power Supply |



Note: Drawings are not to scale.

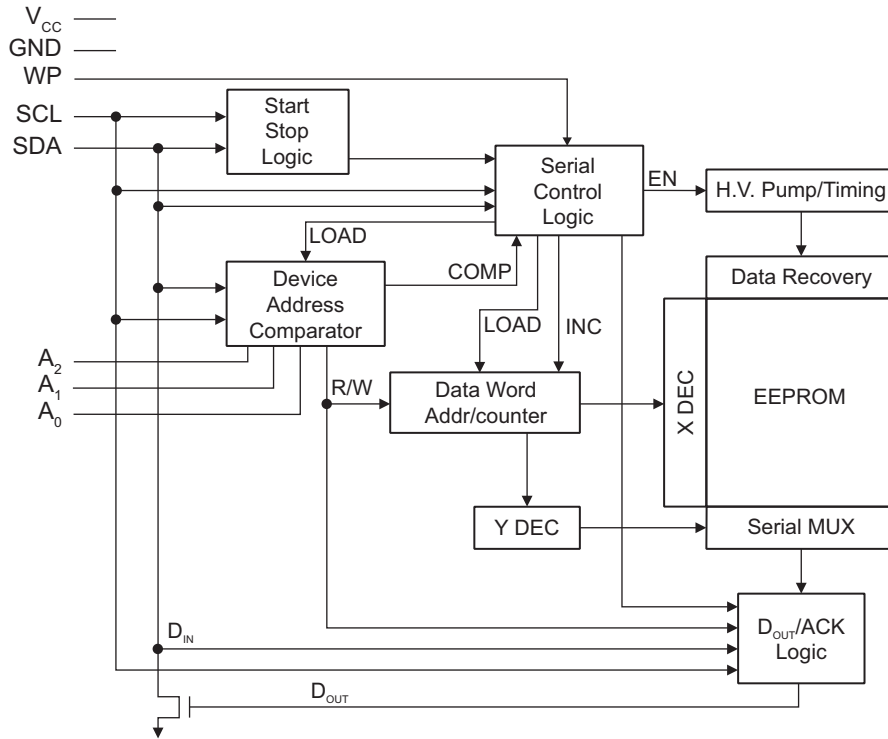
2. Absolute Maximum Ratings

| | |
|--|-----------------|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on any pin with respect to ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0mA |

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pin Descriptions

Serial Clock (SCL) — The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

Serial Data (SDA) — The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven, and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (A₂, A₁, A₀) — The A₂, A₁, and A₀ pins are device address inputs that are hardwired or left not connected for compatibility with other Atmel AT24Cxx devices. When the pins are hardwired, as many as eight 512K devices may be addressed on a single bus system (see Section 7. “Device Addressing” on page 9 for more details). If these pins are left floating, the A₂, A₁, and A₀ pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Write Protect (WP) — The Write Protect input, when connected to GND, allows normal write operations. When WP pin is connected directly to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND; however, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pin to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Table 4-1. Write Protect

| WP Pin Status | Part of the Array Protected |
|--------------------|------------------------------|
| At V _{CC} | Full Array |
| At GND | Normal Read/Write Operations |

5. Memory Organization

AT24C512C, 512-Kbit Serial EEPROM: The 512K is internally organized as 512 pages of 128 bytes each. Random word addressing requires a 16-bit data word address.

5.1 Pin Capacitance

Table 5-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 5.5\text{V}$.

| Symbol | Test Condition | Max | Units | Conditions |
|-----------|---|-----|-------|-----------------------|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O} = 0\text{V}$ |
| C_{IN} | Input Capacitance ($A_0, A_1, A_2, \text{SCL}$) | 6 | pF | $V_{IN} = 0\text{V}$ |

Note: 1. This parameter is characterized and is not 100% tested.

5.2 DC Characteristics

Table 5-2. DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 1.7\text{V}$ to 3.6V or 2.5V to 5.5V (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-----------|---------------------------------|--------------------------------|-------------------------------|------|---------------------|---------------|
| V_{CC1} | Supply Voltage | | 1.7 | | 3.6 | V |
| V_{CC2} | Supply Voltage | | 2.5 | | 5.5 | V |
| I_{CC1} | Supply Current | $V_{CC} = 3.6\text{V}$ | Read at 400kHz | | 1.0 | mA |
| | | | Write at 400kHz | | 3.0 | mA |
| I_{CC2} | Supply Current | $V_{CC} = 5.0\text{V}$ | Read at 400kHz | | 2.0 | mA |
| | | | Write at 400kHz | | 3.0 | mA |
| I_{SB1} | Standby Current | $V_{CC} = 1.7\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 1.0 | μA |
| | | $V_{CC} = 3.6\text{V}$ | | | 3.0 | μA |
| I_{SB2} | Standby Current | $V_{CC} = 2.5\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 2.0 | μA |
| | | $V_{CC} = 5.5\text{V}$ | | | 6.0 | μA |
| I_{LI} | Input Leakage Current | $V_{IN} = V_{CC}$ or V_{SS} | | 0.10 | 3.0 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = V_{CC}$ or V_{SS} | | 0.05 | 3.0 | μA |
| V_{IL} | Input Low Level ⁽¹⁾ | | -0.6 | | $V_{CC} \times 0.3$ | V |
| V_{IH} | Input High Level ⁽¹⁾ | | $V_{CC} \times 0.7$ | | $V_{CC} + 0.5$ | V |
| V_{OL1} | Output Low Level | $V_{CC} = 1.7\text{V}$ | $I_{OL} = 0.15\text{mA}$ | | 0.2 | V |
| V_{OL2} | Output Low Level | $V_{CC} = 3.0\text{V}$ | $I_{OL} = 2.1\text{mA}$ | | 0.4 | V |

Note: 1. V_{IL} min and V_{IH} max are reference only, and are not tested.

5.3 AC Characteristics

Table 5-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.7\text{V}$ to 3.6V or 2.5V to 5.5V (where applicable), $CL = 100\text{pF}$ (unless otherwise noted). Test conditions are listed in [Note 2](#).

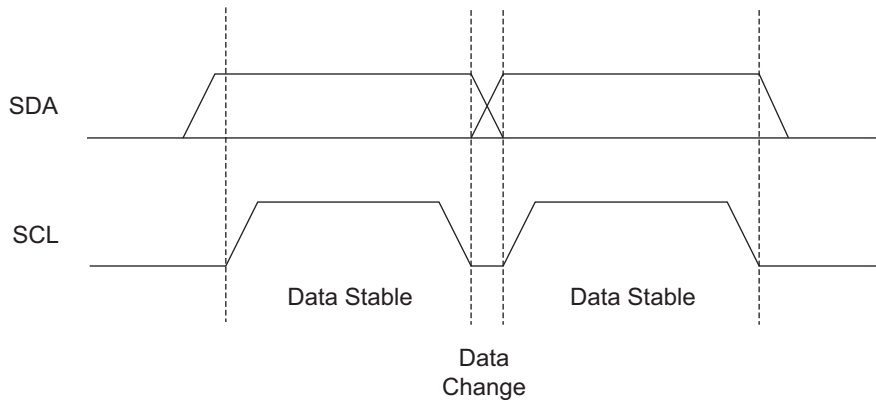
| Symbol | Parameter | 1.7V | | 2.5V, 5.0V | | Units |
|--------------------------|--|-----------|-----|------------|------|---------------|
| | | Min | Max | Min | Max | |
| f_{SCL} | Clock Frequency, SCL | | 400 | | 1000 | kHz |
| t_{LOW} | Clock Pulse Width Low | 1.3 | | 0.4 | | μs |
| t_{HIGH} | Clock Pulse Width High | 0.6 | | 0.4 | | μs |
| t_I | Noise Suppression Time ⁽¹⁾ | | 100 | | 50 | ns |
| t_{AA} | Clock Low to Data Out Valid | 0.05 | 0.9 | 0.05 | 0.55 | μs |
| t_{BUF} | Time the bus must be free before a new transmission can start ⁽¹⁾ | 1.3 | | 0.5 | | μs |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | | 0.25 | | μs |
| $t_{SU.STA}$ | Start Set-up Time | 0.6 | | 0.25 | | μs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | 0 | | μs |
| $t_{SU.DAT}$ | Data In Set-up Time | 100 | | 100 | | ns |
| t_R | Inputs Rise Time ⁽¹⁾ | | 0.3 | | 0.3 | μs |
| t_F | Inputs Fall Time ⁽¹⁾ | | 300 | | 100 | ns |
| $t_{SU.STO}$ | Stop Set-up Time | 0.6 | | 0.25 | | μs |
| t_{DH} | Data Out Hold Time | 50 | | 50 | | ns |
| t_{WR} | Write Cycle Time | | 5 | | 5 | ms |
| Endurance ⁽¹⁾ | 25°C, Page Mode, 3.3V | 1,000,000 | | | | Write Cycles |

- Notes:
- This parameter is ensured by characterization only.
 - AC measurement conditions:
 - R_L (connects to V_{CC}): $1.3\text{k}\Omega$ (2.5V, 5V), $10\text{k}\Omega$ (1.7V)
 - Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
 - Input rise and fall times: $\leq 50\text{ns}$
 - Input and output timing reference voltages: $0.5V_{CC}$

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

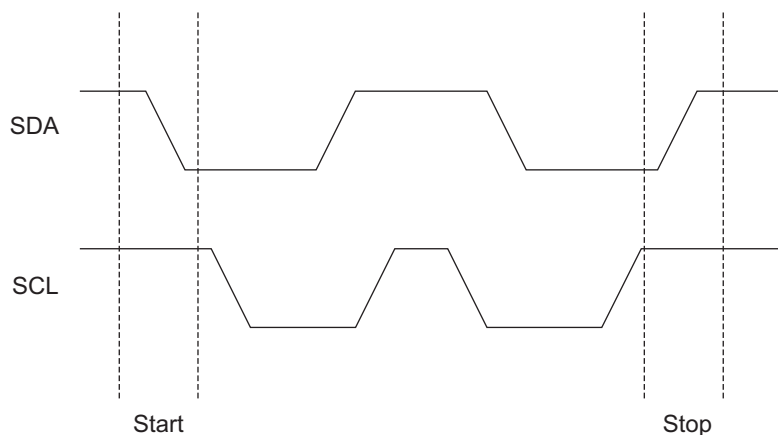
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition, which must precede any other command.

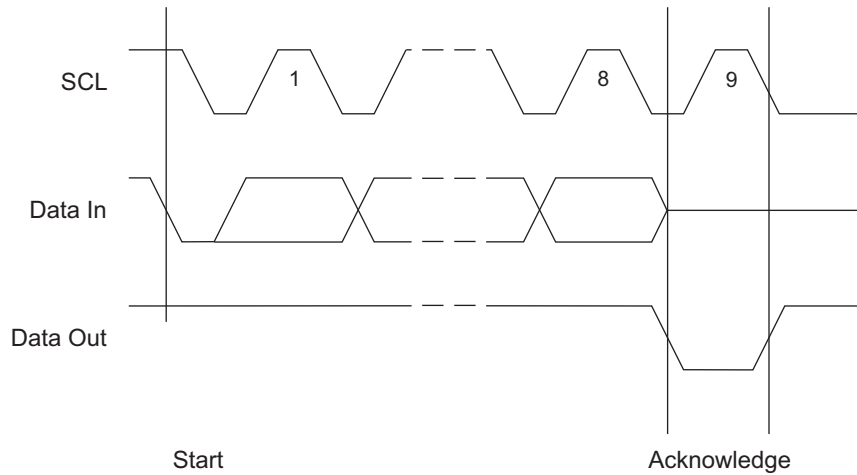
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Figure 6-3. Output Acknowledge



Standby Mode: The AT24C512C features a low-power standby mode, which is enabled:

- Upon power-up and
- After the receipt of the Stop condition and the completion of any internal operations.

Software Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by a Stop condition, as shown in [Figure 6-4](#) below.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 6-4. Software Reset

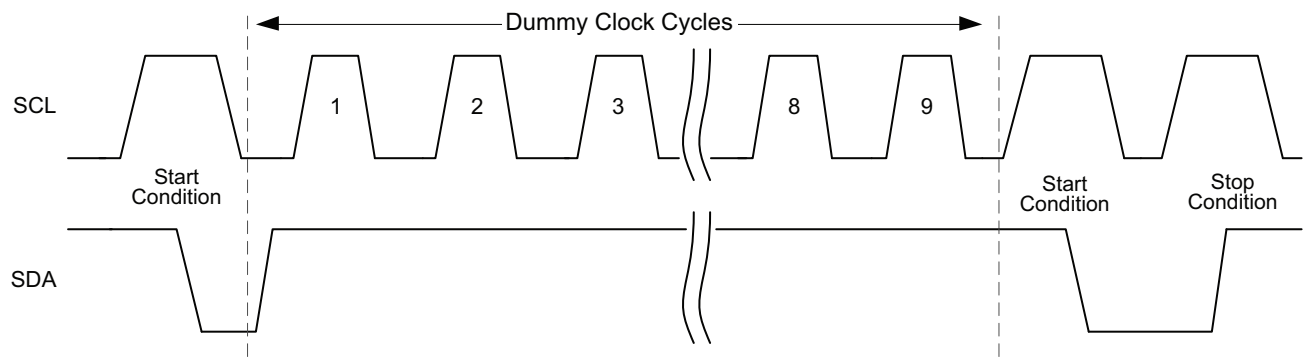


Figure 6-5. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

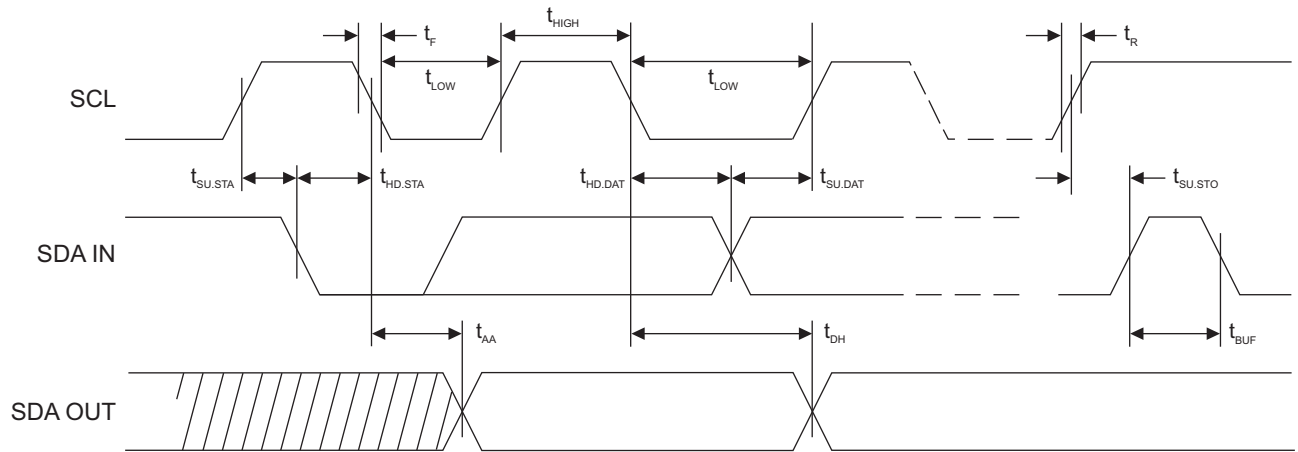
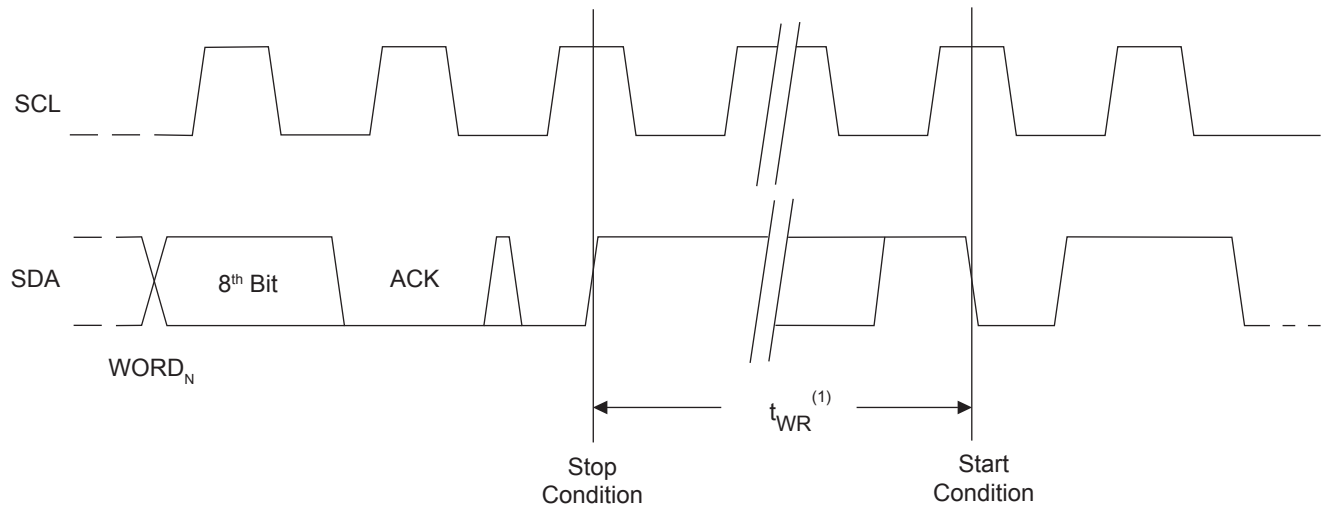


Figure 6-6. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time, t_{WR} , is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

7. Device Addressing

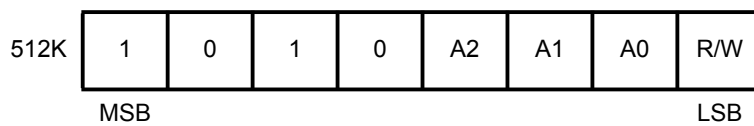
The 512K EEPROM requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation. The device address word consists of a mandatory '1010' sequence for the first four most-significant bits (see Figure 7-1 below). This is common to all 2-wire EEPROM devices.

The 512K uses the three device address bits, A₂, A₁, and A₀, to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A₂, A₁, and A₀ pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a valid compare is not made, the device will return to a standby state.

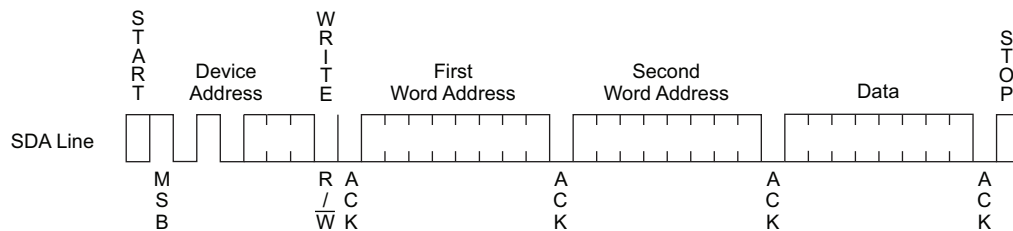
Figure 7-1. Device Address



8. Write Operations

Byte Write: A Byte Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then the part is to receive an 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete (see Figure 8-1).

Figure 8-1. Byte Write

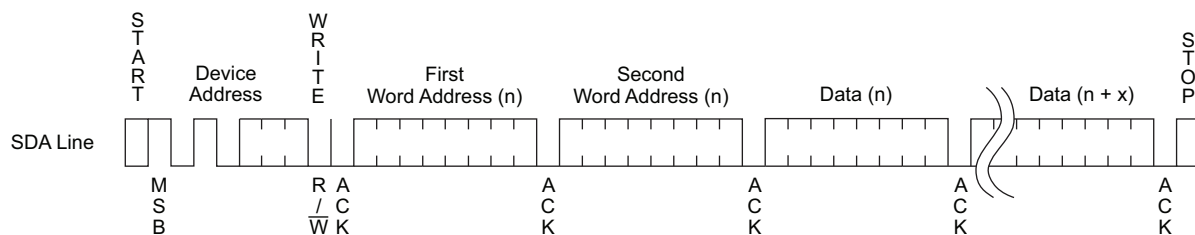


Page Write: The 512-Kbit EEPROM is capable of 128-byte page writes.

A Page Write is initiated the same way as a byte write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition and the internally timed write cycle will begin.

The lower seven bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will roll-over, and the previous data will be overwritten. The address roll over during write is from the last byte of the current page to the first byte of the same page.

Figure 8-2. Page Write



Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write select bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Data Security: AT24C512C has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC} .

9. Read Operations

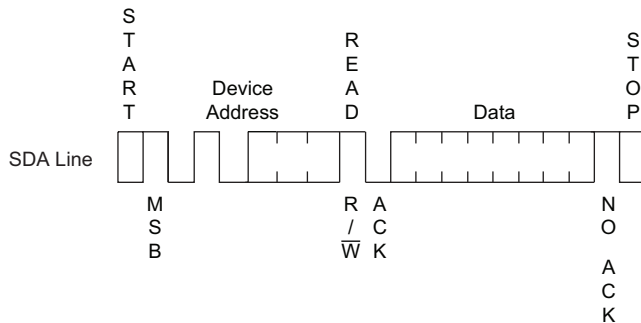
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three types of read operations: Current Address Read, Random Address Read, and Sequential Read.

9.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out on the SDA line. The microcontroller does not respond with a zero, but does generate a following Stop condition.

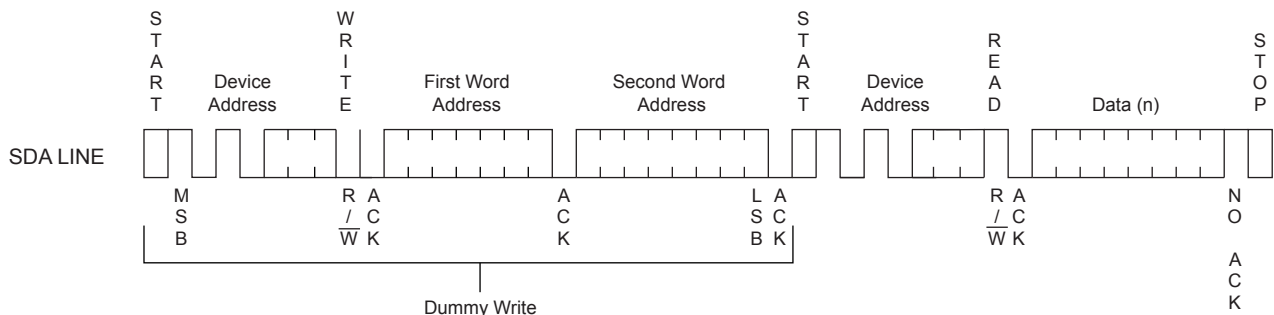
Figure 9-1. Current Address Read



9.2 Random Read

A Random Read requires an initial byte write sequence to load in the data word address. This is known as a “dummy write” operation. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero, but does generate a following Stop condition.

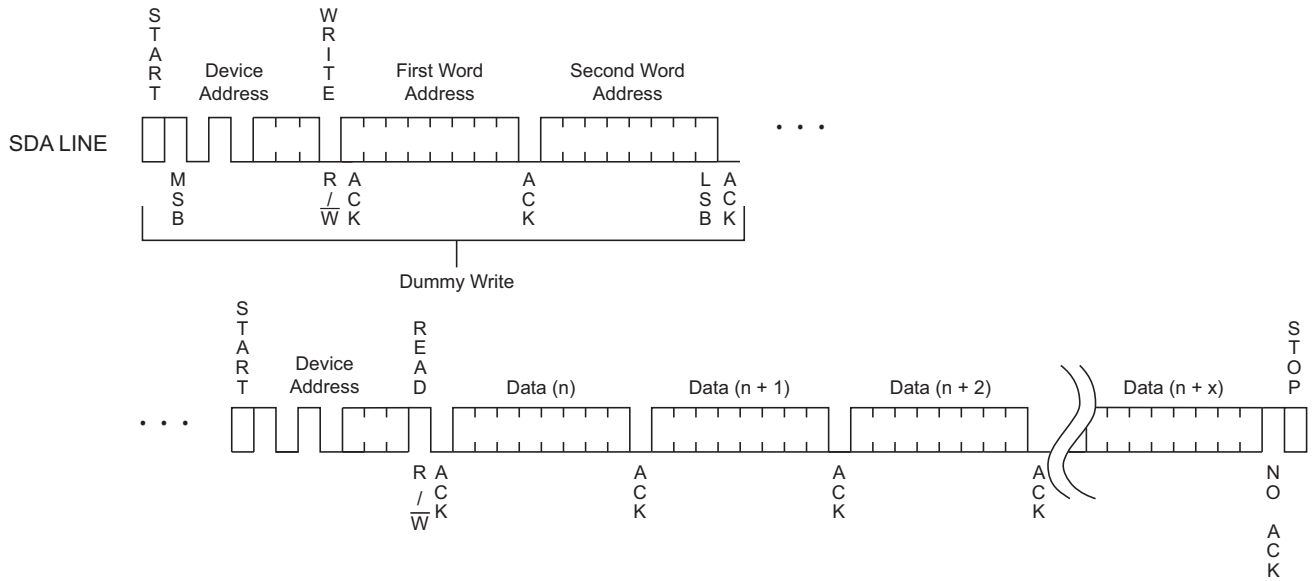
Figure 9-2. Random Read



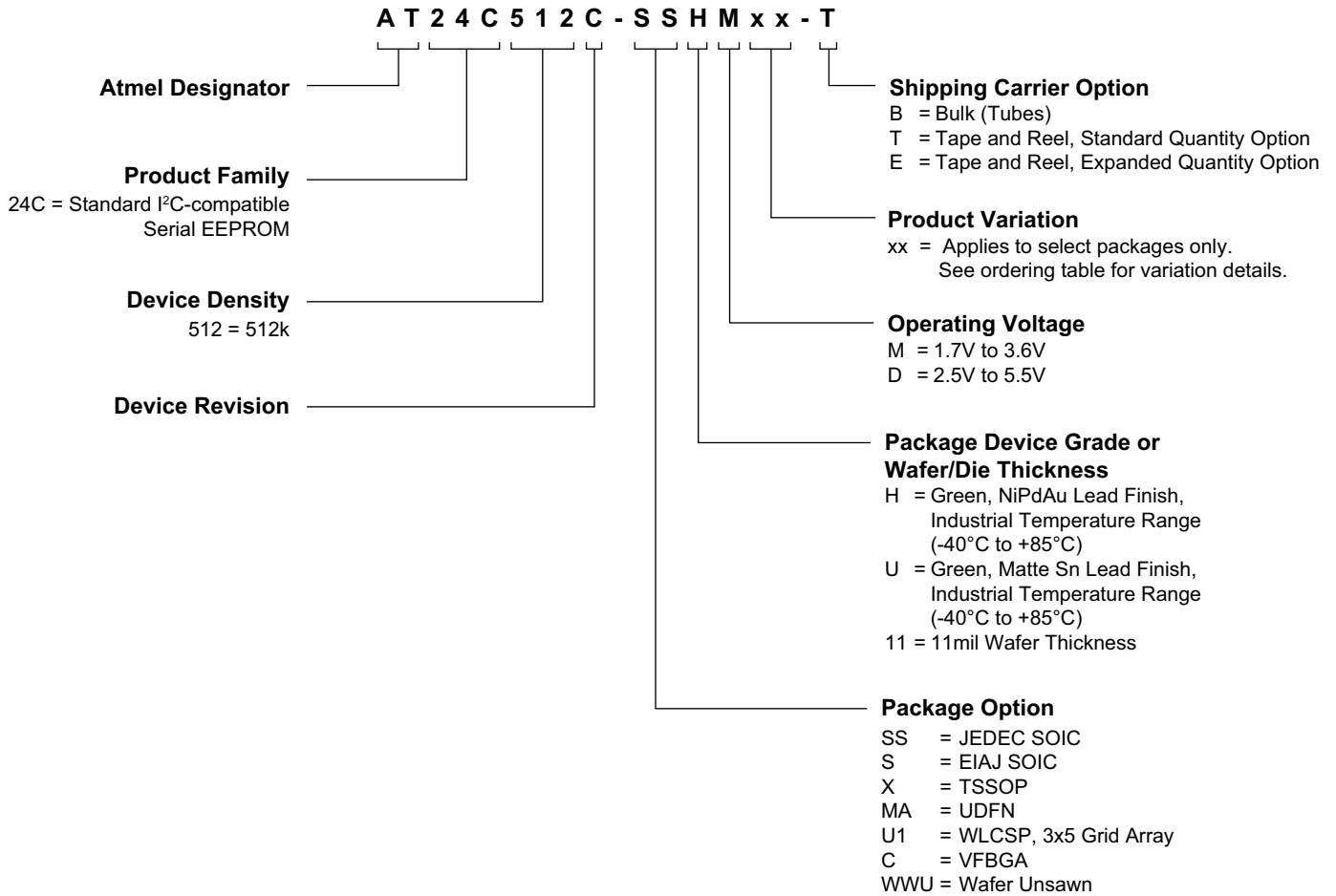
9.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the sequential read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 9-3. Sequential Read

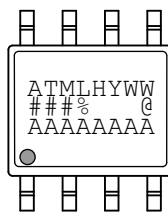
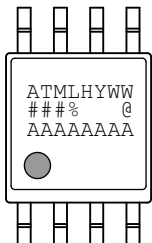

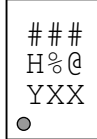
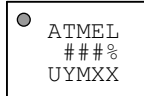
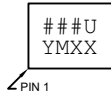


10. Ordering Code Detail



11. Part Markings


AT24C512C: Package Marking Information

| | | |
|---|--|---|
| 8-lead SOIC  | 8-lead EIAJ  | 8-lead TSSOP  |
| 8-pad UDFN 2.0 x 3.0 mm Body  | 8-ball WLCSP  | 8-ball VFBGA 1.5 x 2.0 mm Body  |

Note 1: ● designates pin 1
 Note 2: Package drawings are not to scale

| Catalog Number Truncation | | | |
|--|--|---|---|
| AT24C512C | | Truncation Code: ### = 2FC | |
| Date Codes | | | Voltages |
| Y = Year | M = Month | WW = Work Week of Assembly | % = Minimum Voltage |
| 3: 2013 4: 2014 5: 2015 6: 2016 | 7: 2017 8: 2018 9: 2019 0: 2020 | A: January B: February ... L: December | 02: Week 2 04: Week 4 ... 52: Week 52 |
| M: 1.7V min D: 2.5V min | | | |
| Country of Assembly | | Lot Number | Grade/Lead Finish Material |
| @ = Country of Assembly | | AAA...A = Atmel Wafer Lot Number | H: Industrial/NiPdAu U: Industrial/Matte Tin |
| Trace Code | | | Atmel Truncation |
| XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ | | | AT: Atmel ATM: Atmel ATML: Atmel |

3/25/13

| | | | |
|---|---|-------------|------|
|  Package Mark Contact: DL-CSO-Assy_eng@atmel.com | TITLE | DRAWING NO. | REV. |
| | 24C512CISM, AT24C512C Package Marking Information | 24C512CISM | E |

12. Ordering Information

| Atmel Ordering Code | Lead Finish | Package | Voltage | Delivery Information | | Operation Range | |
|---------------------------------|------------------------------------|------------|----------------|----------------------|----------------|---|-----------------|
| | | | | Form | Quantity | | |
| AT24C512C-SSHM-B | NiPdAu (Lead-free/Halogen-free) | 8S1 | 1.7V to 3.6V | Bulk (Tubes) | 100 per Tube | Industrial Temperature (-40°C to 85°C) | |
| AT24C512C-SSHM-T | | | | Tape and Reel | 4,000 per Reel | | |
| AT24C512C-SSHD-B | | | 2.5V to 5.5V | Bulk (Tubes) | 100 per Tube | | |
| AT24C512C-SSHD-T | | | | Tape and Reel | 4,000 per Reel | | |
| AT24C512C-SHM-B | | 8S2 | 1.7V to 3.6V | Bulk (Tubes) | 95 per Tube | | |
| AT24C512C-SHM-T | | | | Tape and Reel | 2,000 per Reel | | |
| AT24C512C-SHD-B | | | 2.5V to 5.5V | Bulk (Tubes) | 95 per Tube | | |
| AT24C512C-SHD-T | | | | Tape and Reel | 2,000 per Reel | | |
| AT24C512C-XHM-B | | 8X | 1.7V to 3.6V | Bulk (Tubes) | 100 per Tube | | |
| AT24C512C-XHM-T | | | | Tape and Reel | 5,000 per Reel | | |
| AT24C512C-XHD-B | | | 2.5V to 5.5V | Bulk (Tubes) | 100 per Tube | | |
| AT24C512C-XHD-T | | | | | 5,000 per Reel | | |
| AT24C512C-MAHM-T | | | 8MA2 | 1.7V to 3.6V | Tape and Reel | | 5,000 per Reel |
| AT24C512C-MAHM-E | | | | | | | 15,000 per Reel |
| AT24C512C-U1UM-T ⁽¹⁾ | | 8U-8 | 5,000 per Reel | | | | |
| AT24C512C-CUM-T | | 8U2-1 | | | | | |
| AT24C512C-CUMHY-T | | | | | | | |
| AT24C512C-WWU11M ⁽²⁾ | N/A | Wafer Sale | Note 2 | | | | |

- Notes: 1. WLCSP Package: **CAUTION:** Exposure to ultraviolet (UV) light can degrade the data stored in the EEPROM cells. Therefore, customers who use a WLCSP product must ensure that exposure to ultraviolet light does **not** occur
2. For wafer sales, please contact Atmel sales.

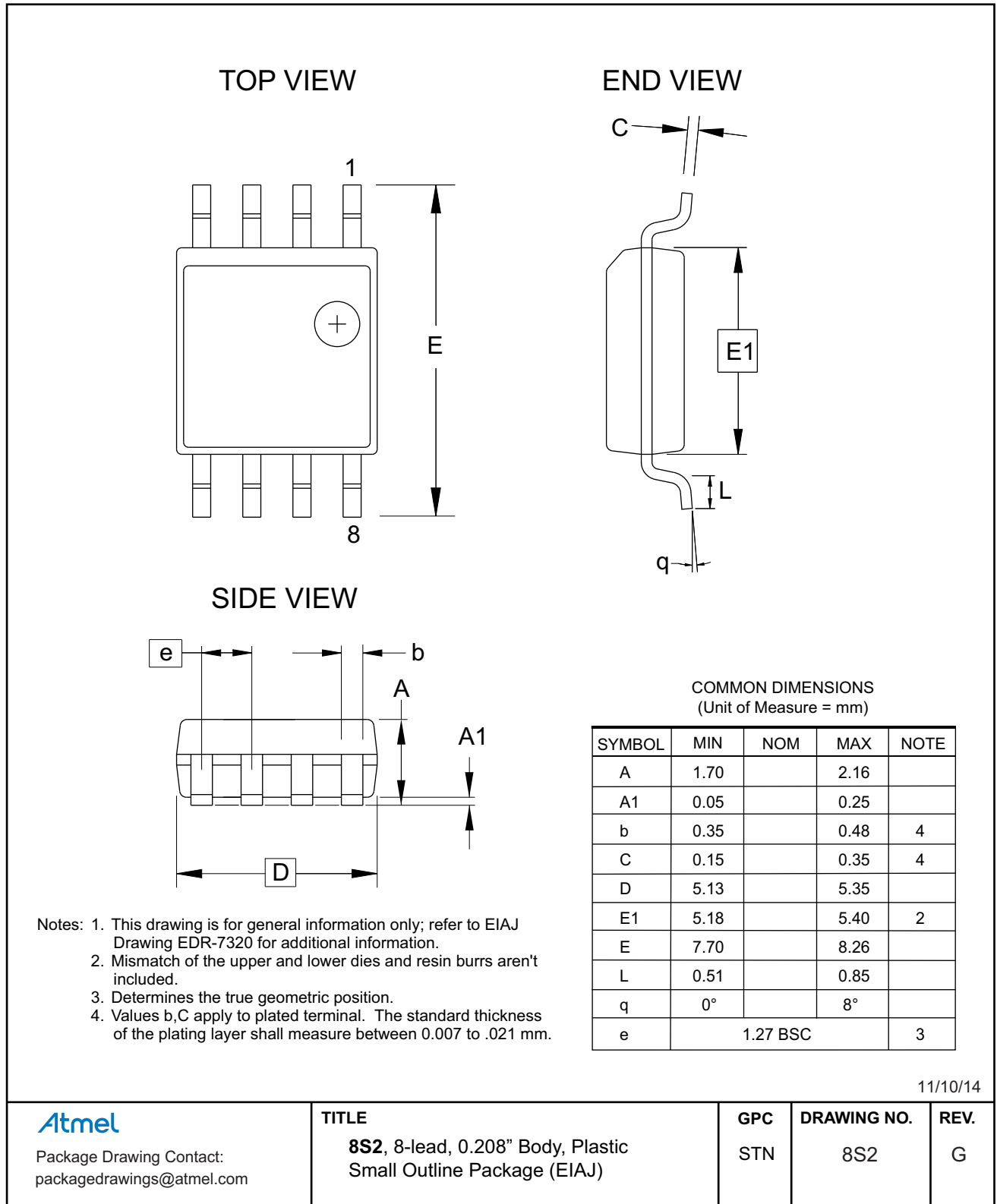
| Package Type | |
|--------------|---|
| 8S1 | 8-lead, 0.150" wide, Plastic Gull Wing, Small Outline (JEDEC SOIC) |
| 8S2 | 8-lead, 0.208" wide, Plastic Gull Wing, Small Outline (EIAJ SOIC) |
| 8X | 8-lead, 4.40mm body, Plastic Thin Shrink Small Outline (TSSOP) |
| 8MA2 | 8-pad, 2.00mm x 3.00mm body, 0.50mm Pitch, Ultra Thin Dual No Lead (UDFN) |
| 8U-8 | 8-ball, 3 x 5 Grid Array, Wafer Level Chip Scale (WLCSP) |
| 8U2-1 | 8-ball, 2.35mm x 3.73mm body, 0.75mm pitch, Small Die Ball Grid Array (VFBGA) |

13. Package Information

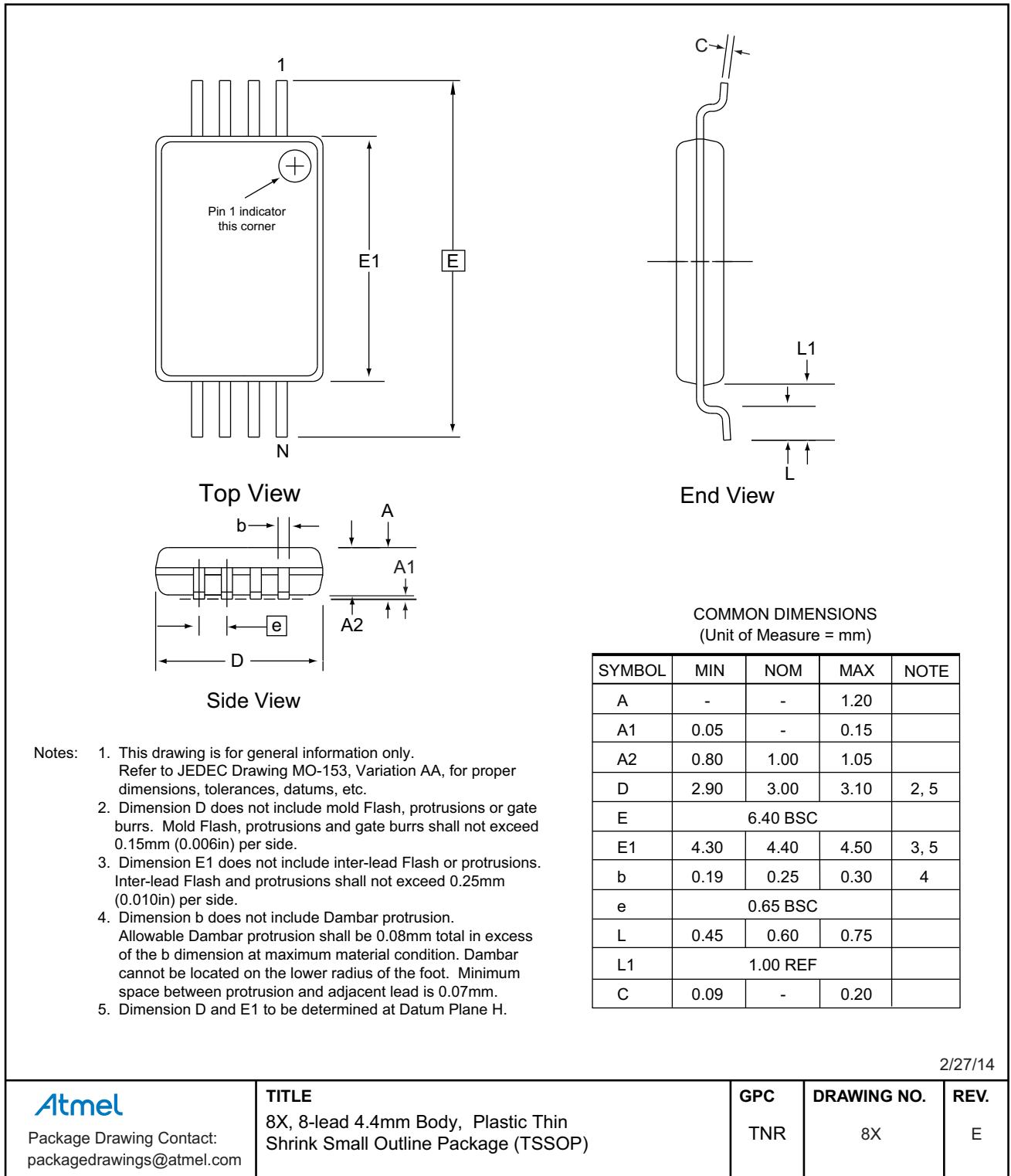
13.1 8S1 — 8-lead JEDEC SOIC



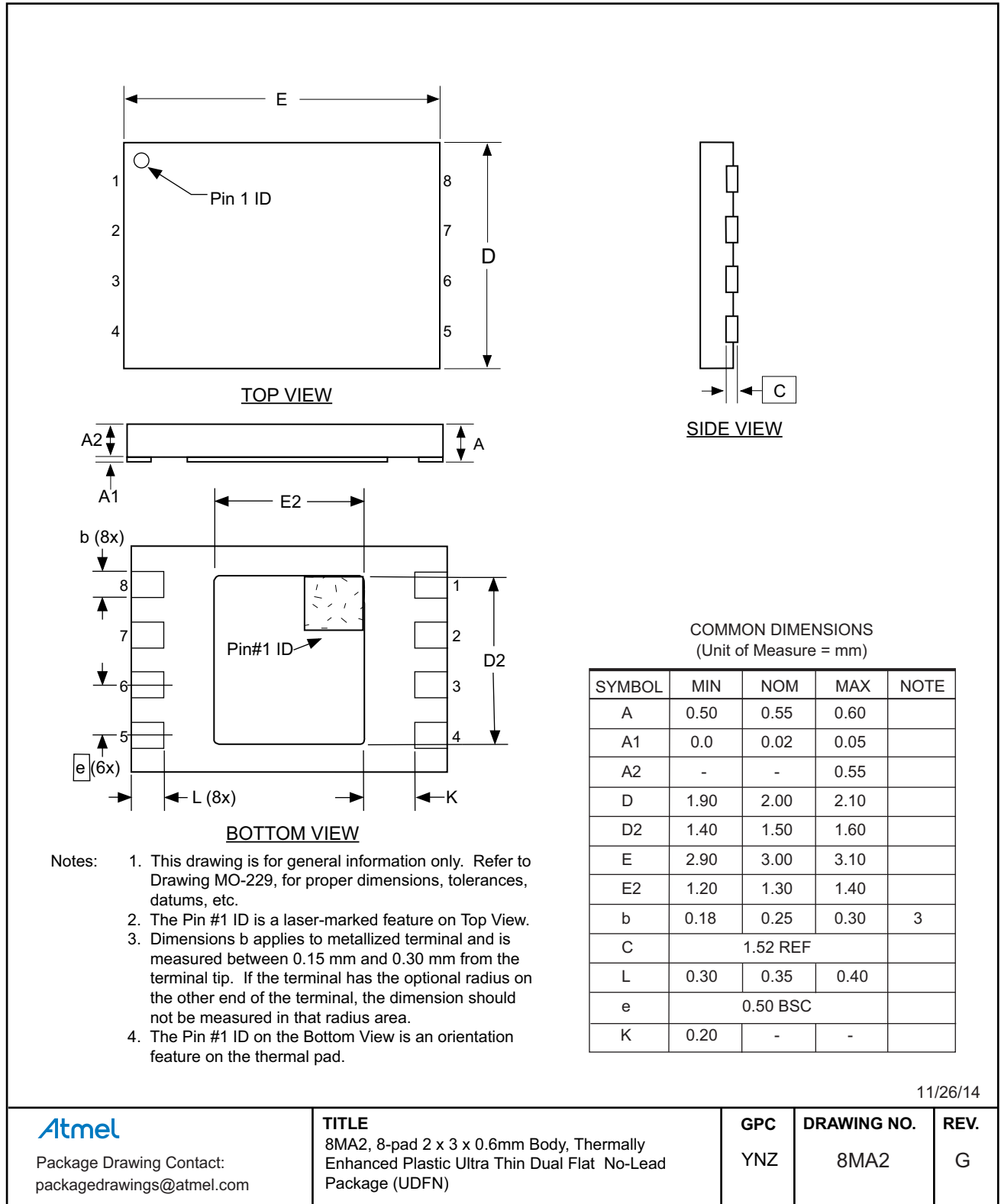
13.2 8S2 — 8-lead EIAJ SOIC



13.3 8X — 8-lead TSSOP



13.4 8MA2 — 8-pad UDFN



11/26/14

Atmel

Package Drawing Contact:
packagedrawings@atmel.com

TITLE

8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)

GPC

YNZ

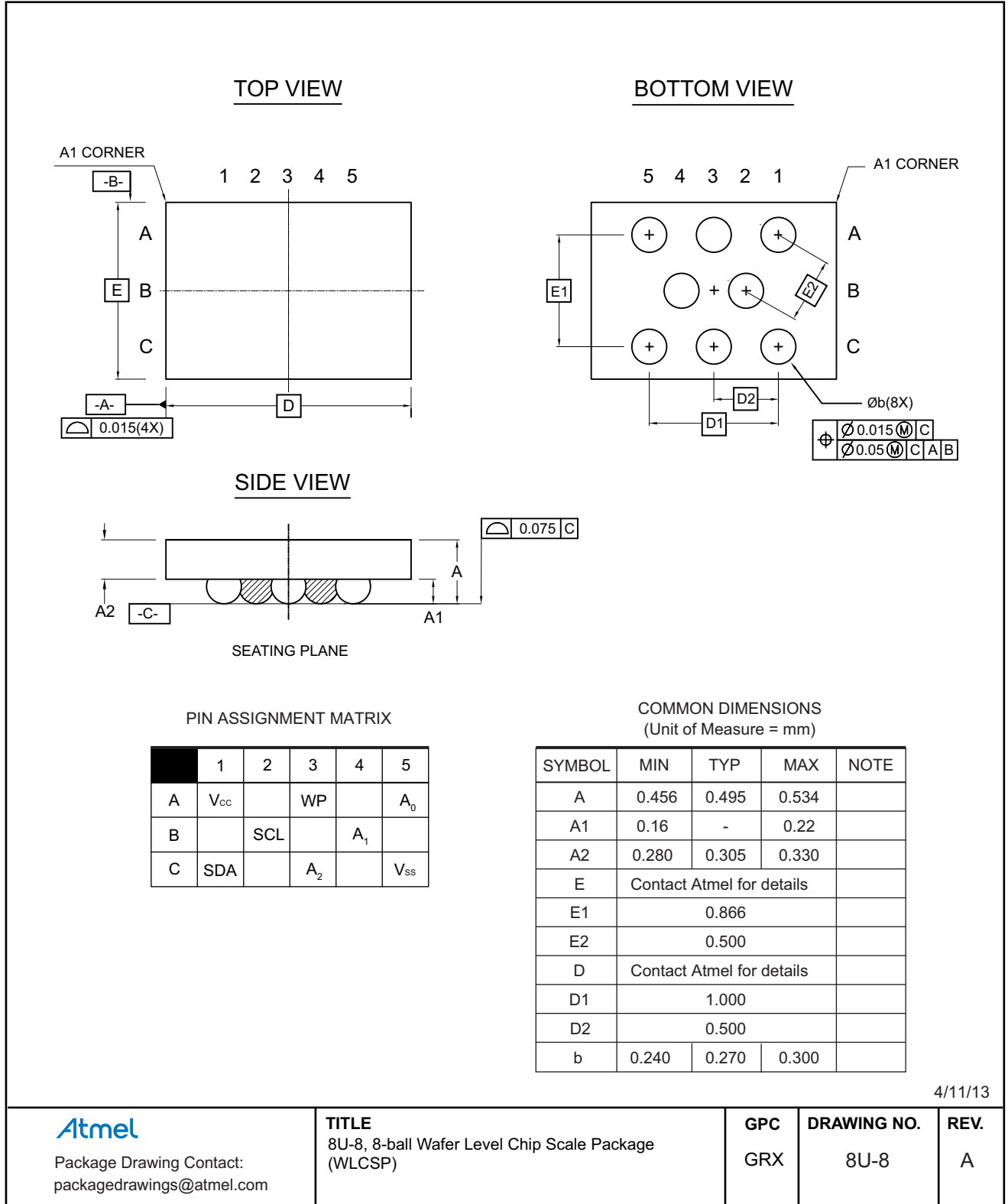
DRAWING NO.

8MA2

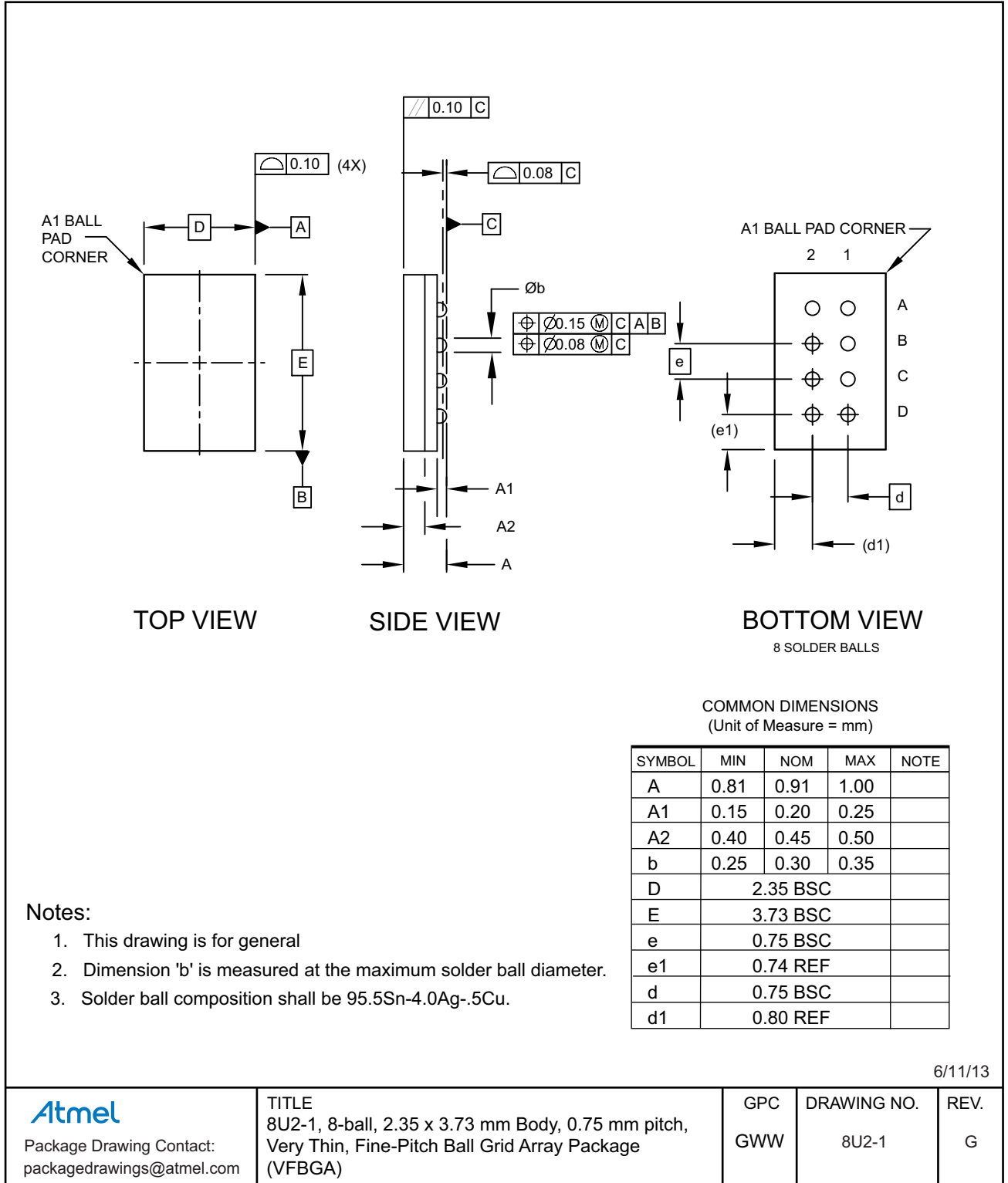
REV.

G

13.5 8U-8 — 8-ball WLCSP



13.6 8U2-1 — 8-ball VFBGA



6/11/13



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
8U2-1, 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch,
Very Thin, Fine-Pitch Ball Grid Array Package
(VFBGA)

GPC
GWW

DRAWING NO.
8U2-1

REV.
G

14. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|---|
| 8720G | 09/2015 | Added the AT24C512C-CUMHY-T package option. |
| 8720F | 01/2015 | Added the UDFN expanded quantity option. Updated package outline drawings and the ordering information section. |
| 8720E | 08/2013 | Correct spelling error. Correct subscript pin names on pinouts. Update the I_{CC1} and I_{CC2} supply currents in the DC Characteristics table. |
| 8720D | 03/2013 | Added 8U-8 WLCSP package offering. Update related information throughout document. Update footers and disclaimer page. |
| 8720C | 07/2012 | Update part markings. Update package drawings. Update template. |
| 8720B | 12/2010 | Replace part markings with single page standard marking. Remove five ordering code variations. |
| 8720A | 09/2010 | Initial document release. |



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