GW1NR series of FPGA products

# Package & Pinout User Guide

**UG119-1.6E, 10/26/2021**

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## Revision History

| Date | Version | Description |
|---|---|---|
| 04/03/2018 | 1.04E | Initial version Published. |
| 06/25/2018 | 1.05E | MG81 package info. Added. |
| 09/13/2018 | 1.06E | The pins distribution view and package outline of MG81added. |
| 12/12/2018 | 1.07E | ● LVDS paris added in Table 2-1;<br>● Packages of the devices embedded with PSRAM added. |
| 01/09/2019 | 1.08E | ● QN88 of GW1NR4 embedded with PSRAM added;<br>● View of pin distribution and I/O bank description updated. |
| 07/09/2019 | 1.09E | The GW1NR-9 MG100 package added. |
| 04/16/2020 | 1.1E | GW1NR-9c added. |
| 05/18/2020 | 1.1.1E | GW1NR-9 MG100PF added. |
| 06/12/2020 | 1.1.2E | GW1NR-9C revised to GW1NR-9. |
| 06/30/2020 | 1.2E | GW1NR-1 added. |
| 07/28/2020 | 1.3E | GW1NR-9 MG100PD added. |
| 09/27/2020 | 1.4E | ● GW1NR-9 MG100PA, MG100PT, and MG100PS added;<br>● GW1NR-9 MG100PD removed. |
| 02/02/2021 | 1.5E | GW1NR-2 MG49P/MG49PG/MG49G added. |
| 10/26/2021 | 1.6E | GW1NR-1 EQ144G and QN48G added. |

# Contents

# List of Figures

# List of Tables

# 1 About This Guide

## 1.1 Purpose

This manual contains an introduction to the GW1NR series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

## 1.2 Related Documents

The latest user guidelines are available on the Gowin website at www.gowinsemi.com:

1. DS117, GW1NR series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG119, GW1NR series of FPGA Products Package and Pinout
4. UG804, GW1NR-1 Pinout
5. UG805, GW1NR-2 Pinout
6. UG116, GW1NR-4 Pinout
7. UG803, GW1NR-9 Pinout

# 1.3 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are delineated in Table 1-1.

**Table 1-1 Abbreviations and Terminologies**

| Abbreviations and Terminology | Full Name |
|---|---|
| FPGA | Field Programmable Gate Array |
| SIP | System in Package |
| SDRAM | Synchronous Dynamic RAM |
| PSRAM | Pseudo Static Random Access Memory |
| GPIO | Gowin Programmable IO |
| FN | QFN |
| QN | QFN |
| MG | MBGA |
| LQ | LQFP |
| EQ | ELQFP |

# 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

# 2 Overview

The GW1NR series of FPGA Products are the first-generation products of GOWINSEMI® (LittleBee®) family. They are available in various forms that offer high I/O compatibility and flexible usage.

## 2.1 PB-Free Package

The GW1NR series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NR series of FPGA products are in full compliance with the IPC-1752 standards.

# 2.2 Package and Max. User I/O Information

**Table 2-1 Package and Max. User I/O Information, LVDS Pairs**

| Package | Pitch(mm) | Size (mm) | GW1NR-1 | GW1NR-2 | GW1NR-4 | GW1NR-9 |
|---|---|---|---|---|---|---|
| FN32G | 0.4 | 4 x 4 | 26 | - | - | - |
| MG49P | 0.5 | 3.8 x 3.8 | - | 30（8） | - | - |
| MG49PG | 0.5 | 3.8 x 3.8 | - | 30（8） | - | - |
| MG49G | 0.5 | 3.8 x 3.8 | - | 30（8） | - | - |
| QN88 | 0.4 | 10 x 10 | - | - | 70(11) | 70（19） |
| QN88P | 0.4 | 10 x 10 | - | - | 70(11) | 70（18） |
| MG81P | 0.5 | 4.5 x 4.5 | - | - | 68(10) | - |
| MG100P | 0.5 | 5 x 5 | - | - | - | 87（16） |
| MG100PF[1] | 0.5 | 5 x 5 | - | - | - | 87（16） |
| MG100PA | 0.5 | 5 x 5 | - | - | - | 87（17） |
| MG100PT | 0.5 | 5 x 5 | - | - | - | 87（17） |
| MG100PS | 0.5 | 5 x 5 | - | - | - | 87（17） |
| LQ144P | 0.5 | 20 x 20 | - | - | - | 120（20） |
| EQ144G | 0.5 | 20 x 20 | 112 | - | - | - |
| QN48G | 0.4 | 6 x 6 | 41 | - | - | - |

**Note!**

- [1]MG100PF: The pinout of ball C1/C2/D2/F1/F9/A7/A6 adjusted on the basis of MG100P;
- In this manual, abbreviations are employed to refer to the package types. See 1.3 Abbreviations and Terminology;
- See GW1NR series Pinouts for more details;
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.

# 2.3 Power Pin

**Table 2-2 Other Pins in the GW1NR Series**

| | | | |
|---|---|---|---|
| VCC | VCCO0 | VCCO1 | VCCO2 |
| VCCO3 | VCCX | VSS | NC |

# 2.4 Pin Quantity

## 2.4.1 Quantity of GW1NR-1 Pins

**Table 2-3 Quantity of GW1NR-1 Pins**

| Pin Type | | GW1NR-1 | | |
|---|---|---|---|---|
| | | FN32G | EQ144G | QN48G |
| I/O Single end/Differential pair[1] | BANK0 | 8/4 | 31/15 | 11/4 |
| | BANK1 | 5/2 | 22/11 | 9/4 |
| | BANK2 | 6/2 | 34/17 | 12/5 |
| | BANK3 | 8/3 | 25/12 | 9/7 |
| Max. User I/O [2] | | 27 | 112 | 41 |
| Differential Pair | | 11 | 55 | 20 |
| VCC | | 1 | 4 | 2 |
| VCCO0 | | 0 | 2 | 0 |
| VCCO1 | | 0 | 3 | 1 |
| VCCO2 | | 1 | 2 | 1 |
| VCCO3 | | 1 | 3 | 0 |
| VCCO0/VCCO1[3] | | 1 | 0 | 0 |
| VCCO0/VCCO3 | | 0 | 0 | 1 |
| VSS | | 1 | 10 | 2 |
| MODE0 | | 0 | 1 | 1 |
| MODE1 | | 0 | 1 | 1 |
| MODE2 | | 0 | 0 | 0 |
| JTAGSEL_N | | 0 | 1 | 0 |
| NC | | 0 | 7 | 0 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.4.2 Quantity of GW1NR-2 Pins

**Table 2-4 Quantity of GW1NR-2 Pins**

| Pin Type | | GW1NR-2 | | |
|---|---|---|---|---|
| | | MG49P | MG49PG | MG49G |
| I/O Single end/Differential pair[1] | BANK0 | 14/7/4 | 14/7/4 | 14/7/4 |
| | BANK1 | 0/0/0 | 0/0/0 | 0/0/0 |
| | BANK2 | 8/4/2 | 8/4/2 | 8/4/2 |
| | BANK3 | 4/2/1 | 4/2/1 | 4/2/1 |
| | BANK4 | 4/2/1 | 4/2/1 | 4/2/1 |
| | BANK5 | 0/0/0 | 0/0/0 | 0/0/0 |
| | BANK6 | 10/5/0 | 10/5/0 | 10/5/0 |
| Max. User I/O [2] | | 40 | 40 | 40 |
| Differential Pair | | 20 | 20 | 20 |
| True LVDS output | | 8 | 8 | 8 |
| VCC | | 1 | 1 | 1 |
| VCCX | | 1 | 1 | 1 |
| VCCO0 | | 1 | 1 | 1 |
| VCCO1 | | 1 | 1 | 1 |
| VCCO2/VCCO3/VCCO4/VCCO5[3] | | 1 | 1 | 1 |
| VCCD | | 1 | 1 | 1 |
| VCCOD | | 1 | 1 | 1 |
| VSS | | 2 | 2 | 2 |
| MODE0 | | 0 | 0 | 0 |
| MODE1 | | 0 | 0 | 0 |
| MODE2 | | 0 | 0 | 0 |
| JTAGSEL_N | | 0 | 0 | 0 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.4.3 Quantity of GW1NR-4 Pins

**Table 2-5 Quantity of GW1NR-4 Pins (SDRAM embedded)**

| Pin Type | | GW1NR-4 |
|---|---|---|
| | | QN88 |
| I/O Single end/Differential pair[1] | BANK0 | 20/5/0 |
| | BANK1 | 15/6/2 |
| | BANK2 | 23/9/7 |
| | BANK3 | 12/4/2 |
| Max. User I/O [2] | | 70 |
| Differential Pair | | 24 |
| True LVDS output | | 11 |
| VCC | | 4 |
| VCCX | | 0 |
| VCCO0 | | 0 |
| VCCO1 | | 1 |
| VCCO2 | | 2 |
| VCCO3 | | 1 |
| VCCX/VCCO0[3] | | 3 |
| VSS | | 6 |
| MODE0 | | 1 |
| MODE1 | | 1 |
| MODE2 | | 0 |
| JTAGSEL_N | | 1 |

**Table 2-6 Quantity of GW1NR-4 Pins (PSRAM embedded)**

| Pin Type | | GW1NR-4 | |
|---|---|---|---|
| | | MG81P | QN88P |
| I/O Single end/Differential pair/LVDS [1] | BANK0 | 13/6/0 | 20/5/0 |
| | BANK1 | 17/3/0 | 15/6/2 |
| | BANK2 | 21/10/10 | 23/9/7 |
| | BANK3 | 17/2/0 | 12/4/2 |
| Max. User I/O[2] | | 68 | 70 |
| Differential Pair | | 21 | 24 |
| True LVDS output | | 10 | 11 |
| VCC | | 3 | 4 |
| VCCX | | 1 | 0 |
| VCCO0 | | 1 | 0 |
| VCCO1 | | 1 | 1 |
| VCCO2 | | 1 | 2 |
| VCCO3 | | 1 | 1 |
| VCCX/VCCO0[3] | | 0 | 3 |
| VSS | | 4 | 6 |
| MODE0 | | 0 | 1 |
| MODE1 | | 1 | 1 |
| MODE2 | | 0 | 0 |
| JTAGSEL_N | | 1 | 1 |

**Note!**

- [1]Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3]Pin multiplexing.

### 2.4.4 Quantity of GW1NR-9 Pins

**Table 2-7 Quantity of GW1NR-9 Pins**

| Pin Type | | GW1NR-9 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | QN88 | QN88P | LQ144P | MG100P | MG100PF | MG100PA | MG100PT | MG100PS |
| I/O Single end/Differential pair/LVDS[1] | BANK0 | 0/0/0 | 0/0/0 | 18/9/0 | 12/6/0 | 12/6/0 | 12/6/0 | 12/6/0 | 12/6/0 |
| | BANK1 | 25/11/4 | 25/11/4 | 32/12/4 | 22/5/1 | 22/6/1 | 22/6/1 | 22/5/1 | 22/6/1 |
| | BANK2 | 23/11/11 | 23/11/11 | 40/19/14 | 32/15/14 | 32/15/14 | 32/15/14 | 32/15/14 | 32/15/14 |
| | BANK3 | 22/8/4 | 22/6/3 | 30/8/2 | 21/4/1 | 21/6/1 | 21/6/2 | 21/4/2 | 21/6/2 |
| Max. User I/O [2] | | 70 | 70 | 120 | 87 | 87 | 87 | 87 | 87 |
| Differential Pair | | 30 | 28 | 48 | 30 | 33 | 33 | 30 | 33 |
| True LVDS output | | 19 | 18 | 20 | 16 | 16 | 17 | 17 | 17 |
| VCC | | 4 | 4 | 4 | 3 | 3 | 3 | 3 | 3 |
| VCCX | | 0 | 0 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCO0 | | 0 | 0 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCO1 | | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCO2 | | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCO3 | | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 |
| VCCX/VCCO0[3] | | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 |
| VSS | | 6 | 6 | 9 | 4 | 4 | 4 | 4 | 4 |
| MODE0 | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| MODE1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| MODE2 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| JTAGSEL_N | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note!**

- [1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

## 2.5 Pin Definitions

The location of the pins in the GW1NR series of FPGA products varies according to the different packages.

Table 2-8 provides a detailed overview of user I/O, multi-function pins, dedicated pins, and other pins.

**Table 2-8 Definition of the Pins in the GW1NR series of FPGA products**

| Pin Name | I/O | Description |
|---|---|---|
| User I/O Pins | | |
| IO[End][Row/Column Number][A/B] | I/O | [End] indicates the pin location, including L (left) R (right) B (bottom), and T (top)<br>[Row/Column Number] indicates the pin Row/Column number. If [End] is T (top) or B (bottom), the pin indicates the column number of the corresponding CFU. If [End] is L (left) or R (right), the pin indicates the Row number of the corresponding CFU.<br>[A/B] indicates differential signal pair information. |
| Multi-Function Pins | | |
| IO[End][Row/Column Number][A/B]/MMM | | /MMM represents one or more of the other functions in addition to being general purpose user I/O. These pins can be used as user I/O when the functions are not used. |
| D0 | I/O | Data port D0 in CPU mode. |
| D1 | I/O | Data port D1 in CPU mode. |
| D2 | I/O | Data port D2 in CPU mode. |
| D3 | I/O | Data port D3 in CPU mode. |
| D4 | I/O | Data port D4 in CPU mode. |
| D5 | I/O | Data port D5 in CPU mode. |
| D6 | I/O | Data port D6 in CPU mode. |
| D7 | I/O | Data port D7 in CPU mode. |
| RECONFIG_N | I, internal weak pull-up | Start new GowinCONFIG mode when low pulse |
| READY | I/O | When high level, the device can be programmed and configured<br>When low level, the device cannot be programmed and configured |
| DONE | I/O | High level indicates successful program and configure<br>Low level indicates incomplete or failed to program and configure |
| FASTRD_N | I/O | In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode. |
| MCLK | I/O | Clock output MCLK in MSPI mode |
| MCS_N5 | I/O | Enable signal MCS_N in MSPI mode, active-low |
| MI | I/O | MI in MSPI mode: Master data input |
| MO | I/O | MO in MSPI mode: Master data output |
| SSPI_CS_N | I/O | Enable signal SSPI_CS_N in SSPI mod, active-low, Internal Weak Pull Up |
| SO | I/O | SO in SSPI mode: Slave data output |
| SI | I/O | SI in SSPI mode: Slave data input |
| TMS | I, internal weak pull-up | Serial mode input in JTAG mode |

| Pin Name | I/O | Description |
|---|---|---|
| TCK | I | Serial clock input in JTAG mode, which needs to be connected with 4.7 K drop-down resistance on PCB |
| TDI | I, internal weak pull-up | Serial data input in JTAG mode |
| TDO | O | Serial data output in JTAG mode |
| JTAGSEL_N | I, internal weak pull-up | Select signal in JTAG mode, active-low |
| SCLK | I | Clock input in SSPI, SERIAL, and CPU mode |
| DIN | I, internal weak pull-up | Input data in SERIAL mode |
| DOUT | O | Output data in SERIAL mode |
| CLKHOLD_N | I, internal weak pull-up | High level, SCLK will be connected internally in SSPI mode or CPU mode<br>Low level, SCLK will be disconnected from SSPI mode or CPU mode |
| WE_N | I | Select data input/output of D[7:0] in CPU mode |
| GCLKT_[x] | I | Pins for global clock input, T(True), [x]: global clock No. |
| GCLKC_[x] | I | Differential comparation input pin of GCLKT_[x], C(Comp), [x]: global clock No. [1] |
| LPLL_T_fb/RPLL_T_fb | I | L/R PLL feedback input pin, T(True) |
| LPLL_C_fb/RPLL_C_fb | I | L/R PLL feedback input pin, C(Comp) |
| LPLL_T_in/RPLL_T_in | I | L/R PLL clock input pin, T(True) |
| LPLL_C_in/RPLL_C_in | I | L/R PLL clock input pin, C(Comp) |
| MODE2 | I, internal weak pull-up | GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded. |
| MODE1 | I, internal weak pull-up | GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded. |
| MODE0 | I, internal weak pull-up | GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded. |
| SDA | I/O | $I^2C$ serial data line |
| SCL | I | $I^2C$ serial clock line |
| Other Pins | | |
| CKP | DIO[2] | Clock channel input pin for MIPI_DPHY_RX, T(True) |
| CKN | DIO[2] | Differential comparison input pin of clock channel for MIPI_DPHY_RX, C(Comp) |
| RX0P | DIO[2] | Data channel 0 input pin for MIPI_DPHY_RX, T(True) |
| RX0N | DIO[2] | Differential comparison input pin of data channel 0 for MIPI_DPHY_RX, C(Comp) |
| RX1P | DIO[2] | Data channel 1 input pin for MIPI_DPHY_RX, T(True) |
| RX1N | DIO[2] | Differential comparison input pin of data channel 1 for MIPI_DPHY_RX, C(Comp) |
| RX2P | DIO[2] | Data channel 2 input pin for MIPI_DPHY_RX, T(True) |
| RX2N | DIO[2] | Differential comparison input pin of data channel 2 for MIPI_DPHY_RX, C(Comp) |

| Pin Name | I/O | Description |
|---|---|---|
| RX3P | DIO[2] | Data channel 3 input pin for MIPI_DPHY_RX, T(True) |
| RX3N | DIO[2] | Differential comparison input pin of data channel 3 for MIPI_DPHY_RX, C(Comp) |
| NC | NA | Reserved. |
| VSS | NA | Ground pins |
| VCC | NA | Power supply pins for internal core logic. |
| VCCO# | NA | Power supply pins for the I/O voltage of I/O BANK#. |
| VCCX | NA | Power supply pins for auxiliary voltage. |

**Note!**

- [1] When the input is not single-ended, the GLKC_[x] pin is not a global clock pin.
- [2] DIO is a dedicated pin.

# 2.6 Introduction to the I/O BANK

GW1NR-1/4/9 includes four I/O Banks.

GW1NR-2 MG49P/MG49PG/MG49G includes seven I/O Banks.

This manual provides an overview of the distribution view of the pins in the GW1NR series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different IO Banks in the GW1NR series FPGA products are marked with different colors.

User I/O, power, and ground are also marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

- “  ” denotes I/Os in BANK0.
- ”  ” denotes I/Os in BANK1.
- ”  ” denotes I/Os in BANK2.
- ”  ” denotes I/Os in BANK3.
- ”  ” denotes I/Os in BANK4.
- ”  ” denotes I/Os in BANK5.
- ”  ” denotes I/Os in BANK6.
- “  ” denotes VCC, VCCX, and VCCO. The filling color does not change.
- ”  ” denotes VCC. The filling color does not change.
- “  ” denotes NC.

# 3 View of Pin Distribution

## 3.1 View of GW1NR-1 Pins Distribution

### 3.1.1 View of FN32G Pins Distribution

**Figure 3-1 View of GW1NR-1 FN32G Pins Distribution (Top View)**

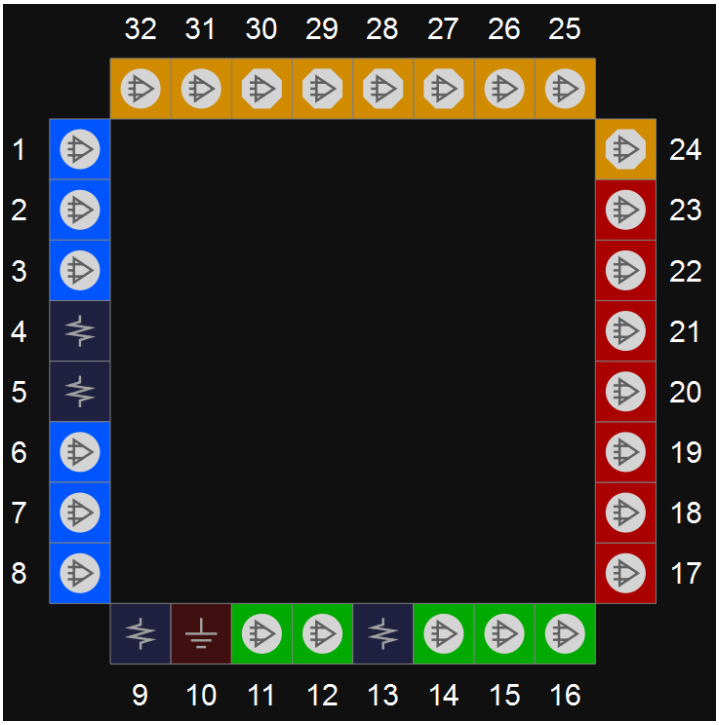



**Table 3-1 Other pins in GW1NR-1 FN32G**

| | |
|---|---|
| VCC | 9 |
| VCCO0/VCCO1 | 13 |
| VCCO2 | 5 |
| VCCO3 | 4 |
| VSS | 10 |

## 3.1.2 View of EQ144G Pins Distribution

**Figure 3-2 View of GW1NR-1 EQ144G Pins Distribution (Top View)**


**Table 3-2 Other pins in GW1NR-1 EQ144G**

| | |
|---|---|
| VCC | 1,36,73,108 |
| VCCO0 | 109,127 |
| VCCO1 | 77,91,103 |
| VCCO2 | 37,55 |
| VCCO3 | 5,19,31 |
| VSS | 2,35,74,107,125,89,105,53,17,33 |
| NC | 93,94,95,96,110,111,112 |

### 3.1.3 View of QN48G Pins Distribution

**Figure 3-3 View of GW1NR-1 QN48G Pins Distribution (Top View)**

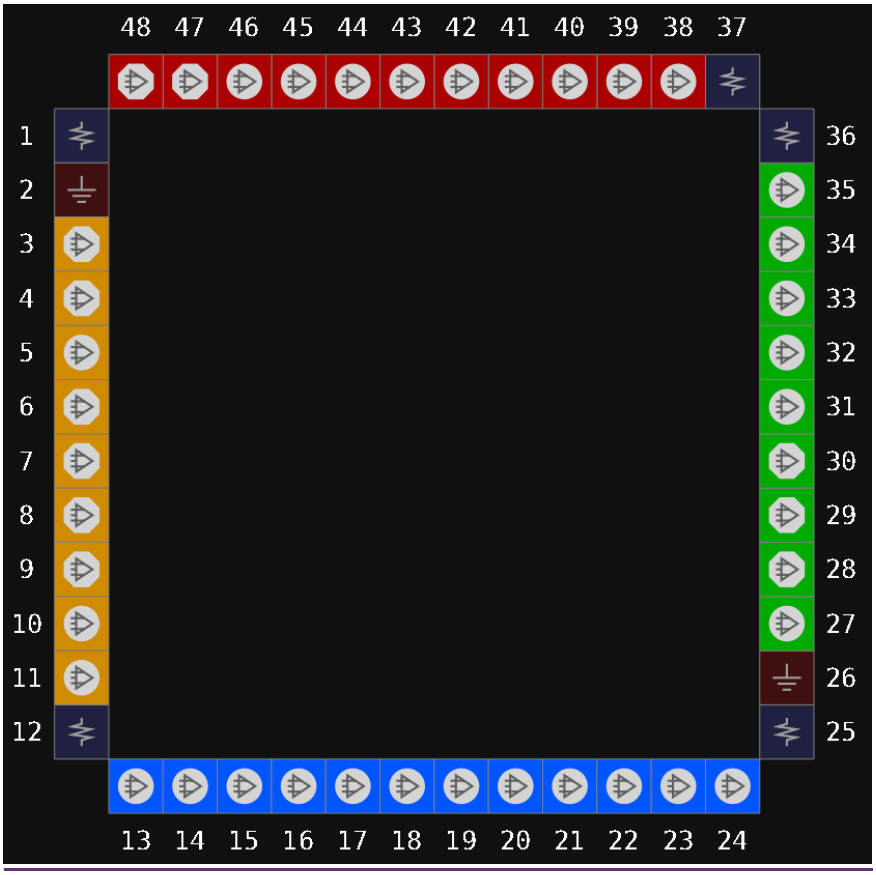



**Table 3-3 Other pins in GW1NR-1 QN48G**

| | |
|---|---|
| VCC | 12,37 |
| VCCO1 | 36 |
| VCCO2 | 25 |
| VCCO0/VCCO3 | 1 |
| VSS | 2,26 |

# 3.2 View of GW1NR-2 Pins Distribution

## 3.2.1 View of MG49P Pins Distribution (PSRAM Embedded)

**Figure 3-4 View of GW1NR-2 MG49P Pins Distribution (Top View, PSRAM Embedded)**

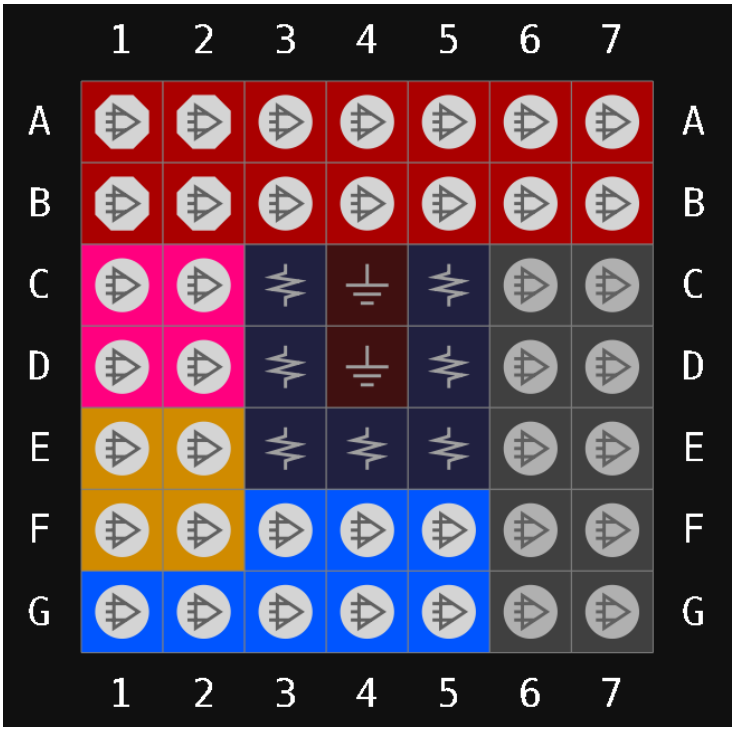



**Table 3-4 Other pins in GW1NR-2 MG49P (PSRAM Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCOD | E5 |
| VCCO0 | C5 |
| VCCO1 | D5 |
| VCCO2/VCCO3/VCCO4/VCCO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

### 3.2.2 View of MG49PG Pins Distribution (PSRAM and Flash Embedded)

**Figure 3-5 View of GW1NR-2 MG49PG Pins Distribution (Top View, PSRAM and Flash Embedded)**

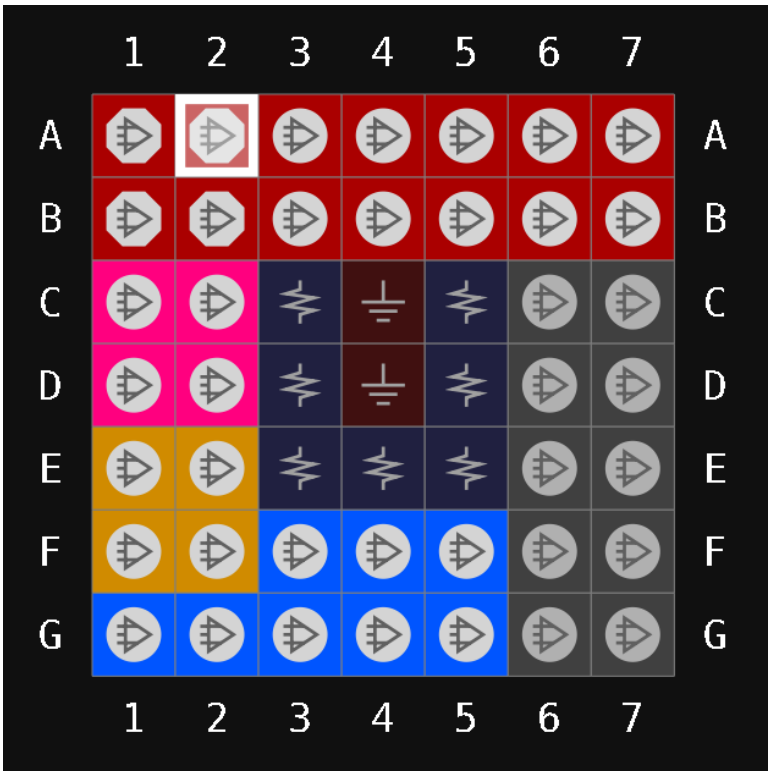



**Table 3-5 Other pins in GW1NR-2 MG49PG (PSRAM and Flash Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCOD | E5 |
| VCCO0 | C5 |
| VCCO1 | D5 |
| VCCO2/VCCO3/VCCO4/VCCO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

### 3.2.3 View of MG49G Pins Distribution (Flash Embedded)

**Figure 3-6 View of GW1NR-2 MG49G Pins Distribution (Top View, Flash Embedded)**

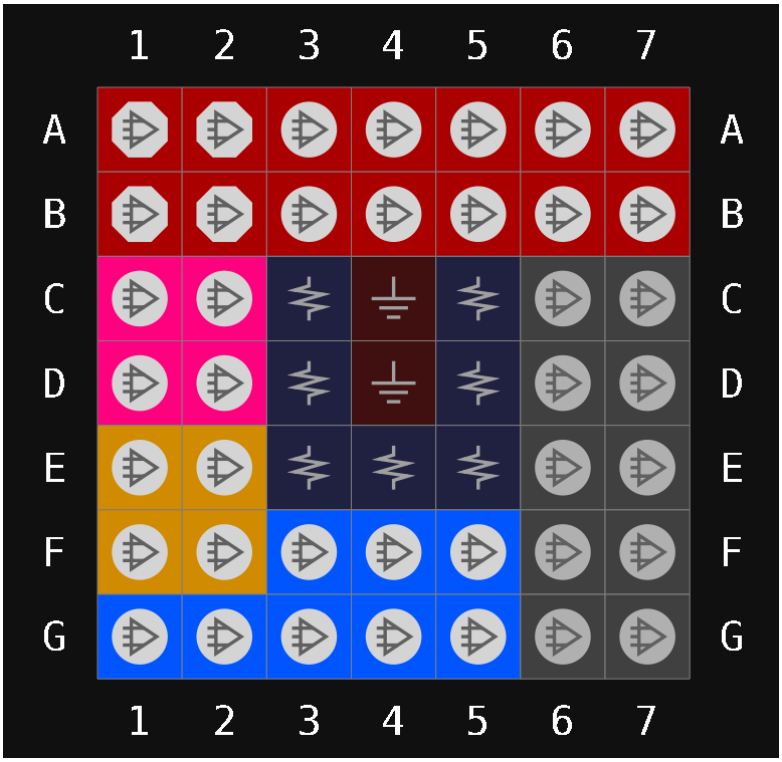



**Table 3-6 Other pins in GW1NR-2 MG49G (Flash Embedded)**

| | |
|---|---|
| VCC | C3 |
| VCCD | E4 |
| VCCOD | E5 |
| VCCO0 | C5 |
| VCCO1 | D5 |
| VCCO2/VCCO3/VCCO4/VCCO5 | D3 |
| VCCX | E3 |
| VSS | C4,D4 |

# 3.3 View of GW1NR-4 Pins Distribution

## 3.3.1 View of MG81P Pins Distribution (PSRAM Embedded)

**Figure 3-7 View of GW1NR-4 MG81P Pins Distribution (Top View, PSRAM Embedded)**

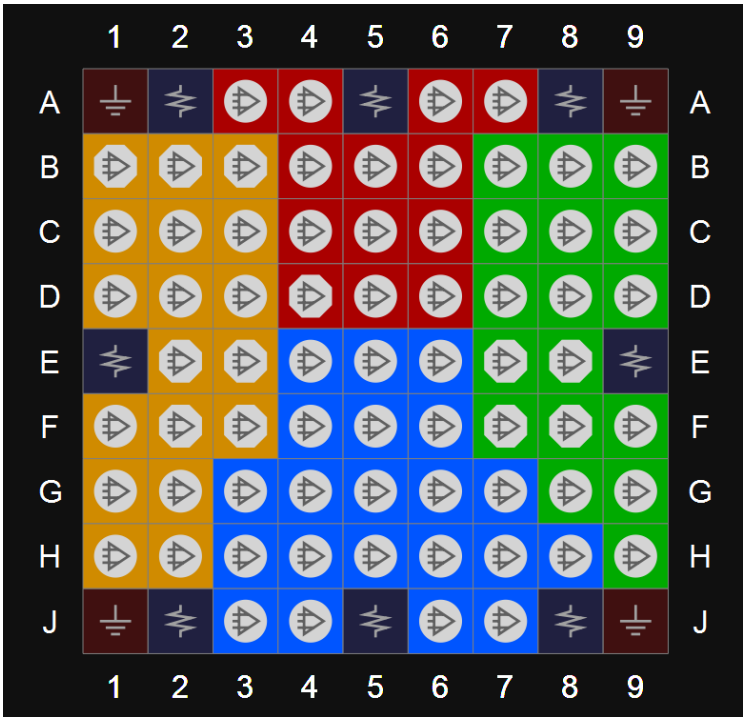



**Table 3-7 Other pins in GW1NR-4 MG81P (PSRAM Embedded)**

| | |
|---|---|
| VCC | A2, A8, J2 |
| VCCX | J8 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VSS | A1, A9, J1, J9 |

## 3.3.2 View of QN88P Pins Distribution (PSRAM Embedded)

**Figure 3-8 View of GW1NR-4 QN88P Pins Distribution (Top View, PSRAM Embedded)**

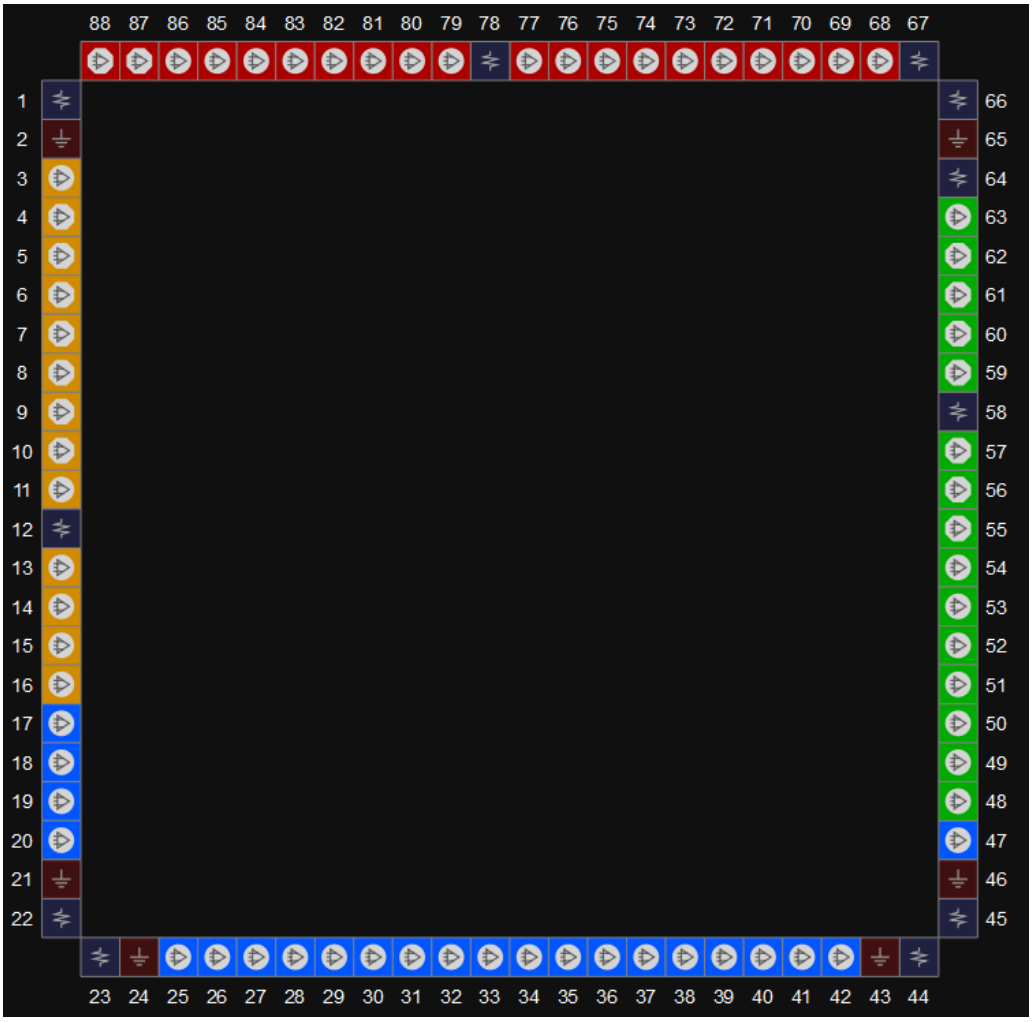



**Table 3-8 Other pins in GW1NR-4 QN88P (PSRAM Embedded)**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCO0 | 64, 67, 78 |
| VCCO1 | 58 |
| VCCO2 | 23, 44 |
| VCCO3 | 12 |
| VSS | 2, 21, 24, 43, 46, 65 |

### 3.3.3 View of QN88 Pins Distribution (SDRAM Embedded)

**Figure 3-9 View of GW1NR-4 QN88 Pins Distribution (Top View, SDRAM Embedded)**

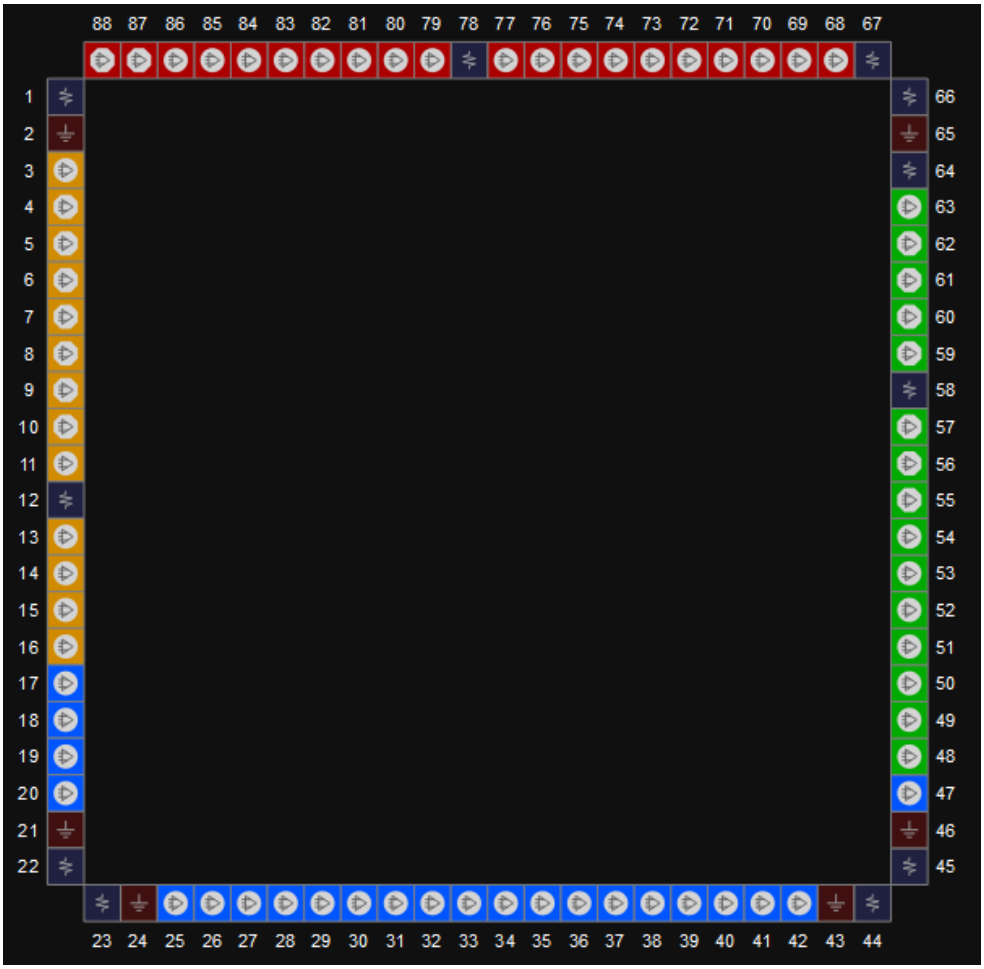



**Table 3-9 Other pins in GW1NR-4 QN88 (SDRAM Embedded)**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCO0 | 64, 67, 78 |
| VCCO1 | 58 |
| VCCO2 | 23, 44 |
| VCCO3 | 12 |
| VSS | 2, 21, 24, 43, 46, 65 |

# 3.4 View of GW1NR-9 Pins Distribution

## 3.4.1 View of QN88 Pins Distribution

**Figure 3-10 View of GW1NR-9 QN88 Pins Distribution (Top View)**

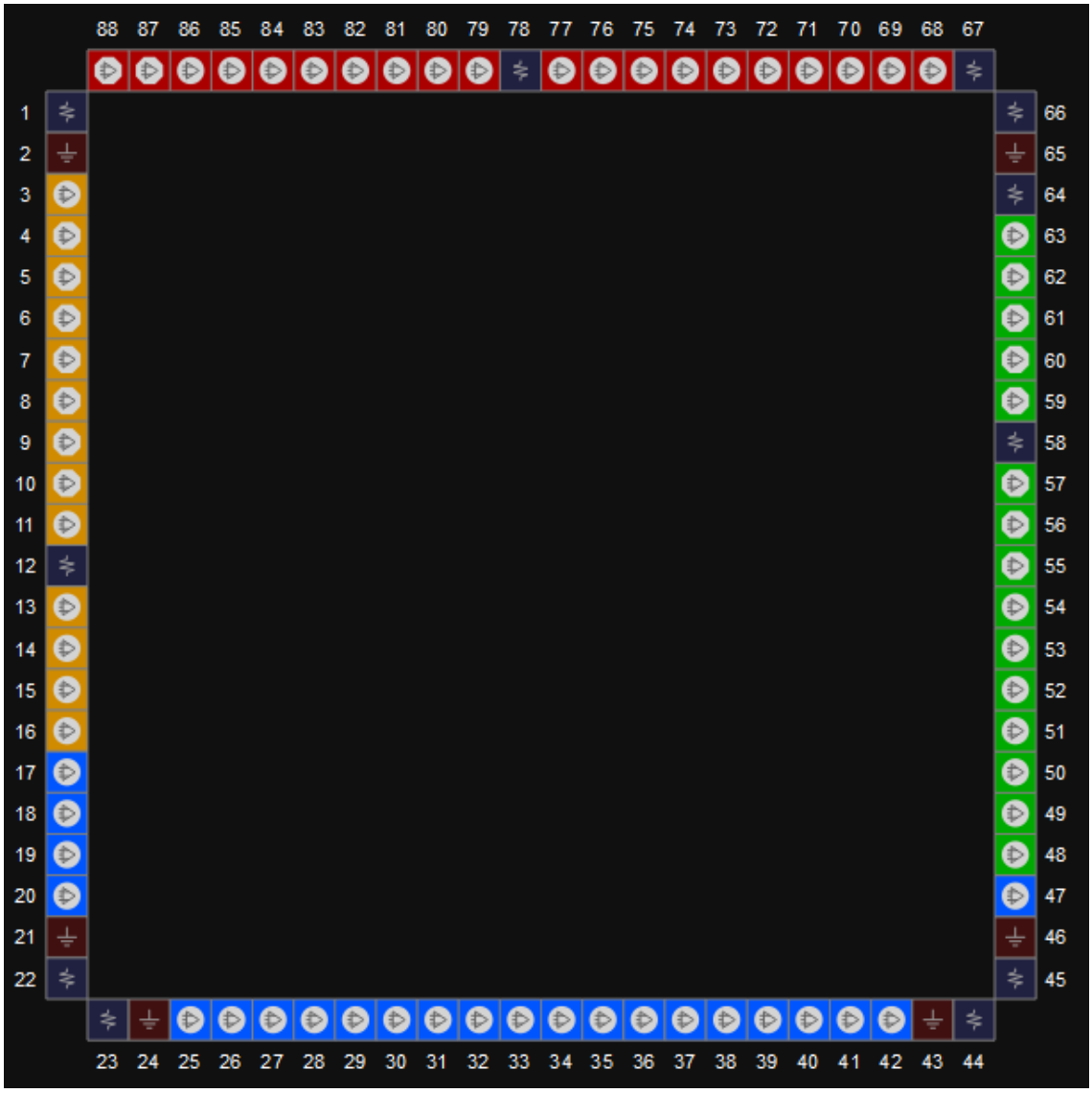



**Table 3-10 Other pins in GW1NR-9 QN88**

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCO0 | 64, 67, 78 |
| VCCO1 | 58 |
| VCCO2 | 23, 44 |
| VCCO3 | 12 |
| MODE | 87, 88 |
| VSS | 2, 21, 24, 43, 46, 65 |

## 3.4.2 View of QN88P Pins Distribution

Figure 3-11 View of GW1NR-9 QN88P Pins Distribution (Top View)

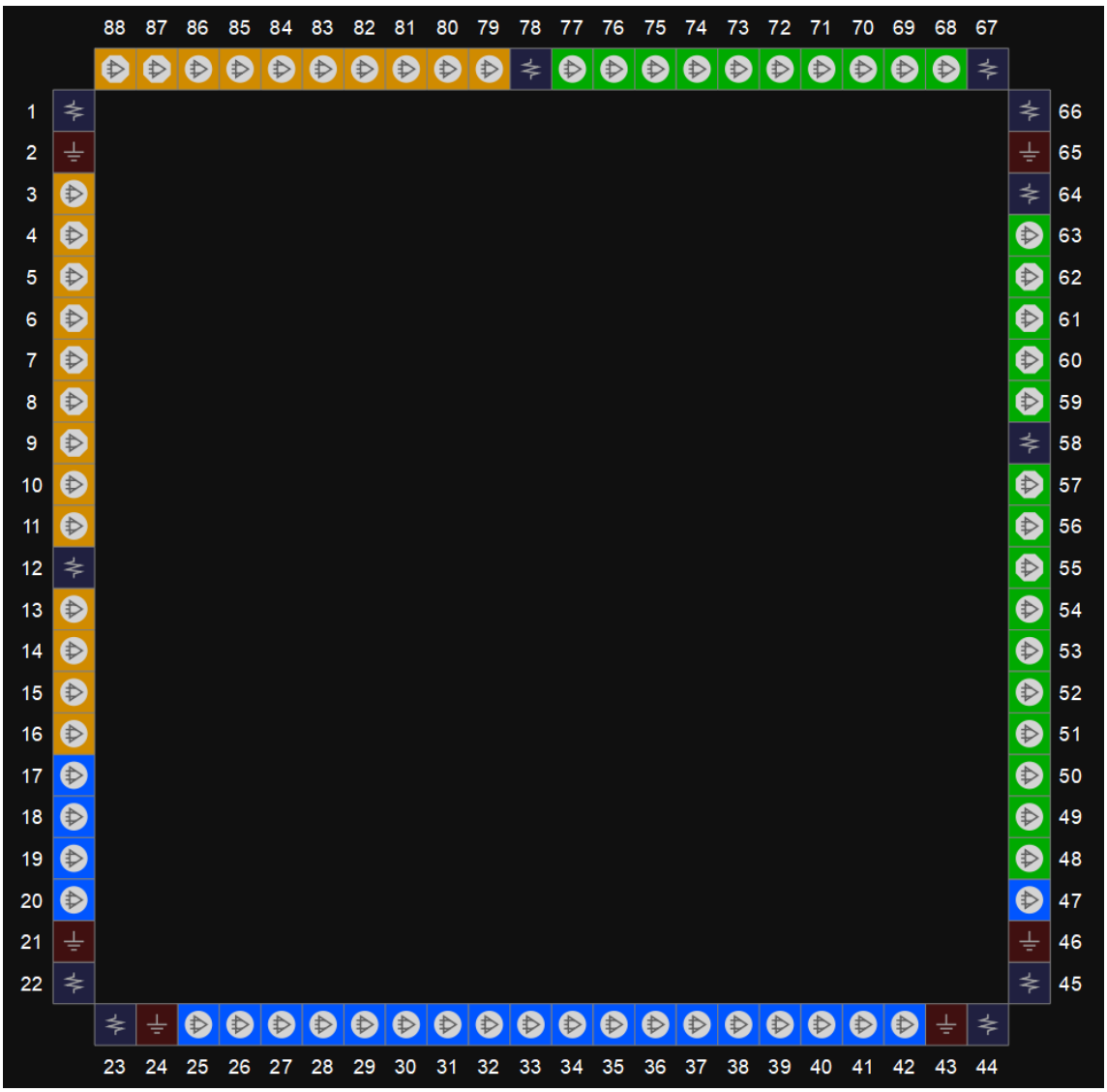



Table 3-11 Other pins in GW1NR-9 QN88P

| | |
|---|---|
| VCC | 1, 22, 45, 66 |
| VCCX/VCCO0 | 64, 67, 78 |
| VCCO1 | 58 |
| VCCO2 | 23, 44 |
| VCCO3 | 12 |
| MODE | 87, 88 |
| VSS | 2, 21, 24, 43, 46, 65 |

### 3.4.3 View of MG100P Pins Distribution

**Figure 3-12 View of GW1NR-9 MG100P Pins Distribution (Top View)**

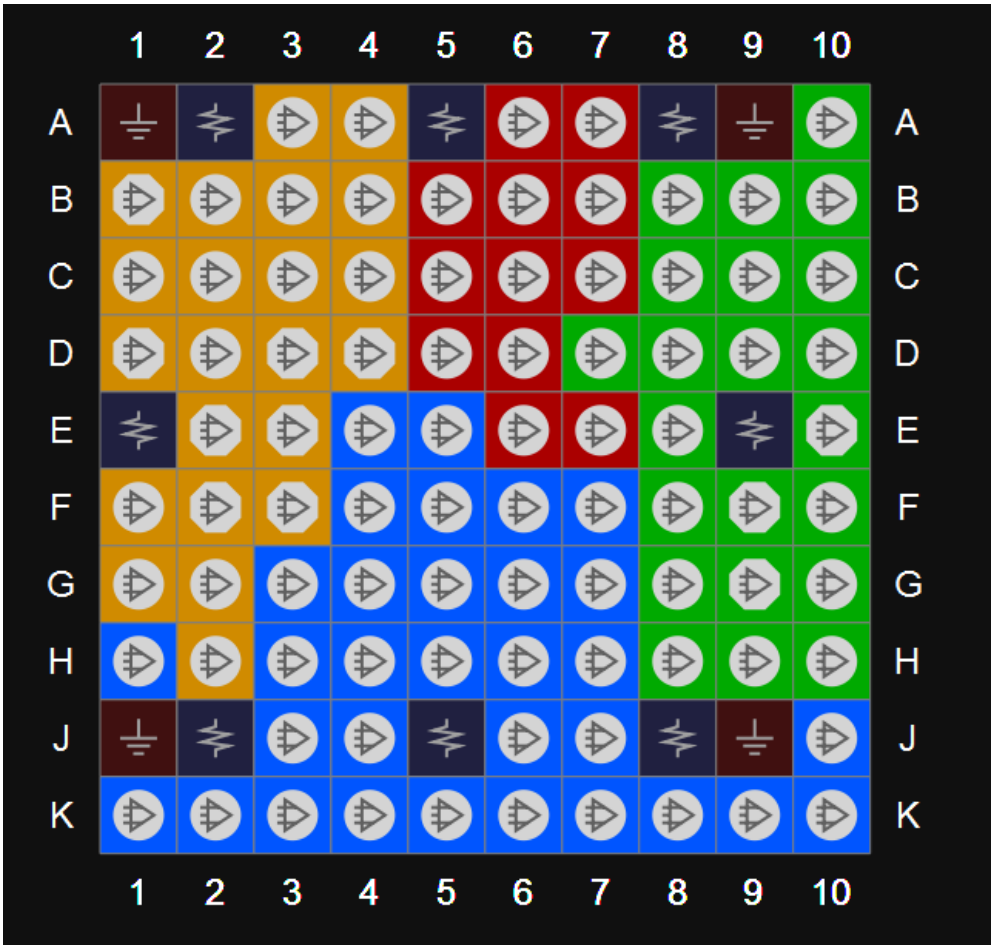



**Table 3-12 Other pins in GW1NR-9 MG100P**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

### 3.4.4 View of MG100PF Pins Distribution

**Figure 3-13 View of GW1NR-9 MG100PF Pins Distribution (Top View)**

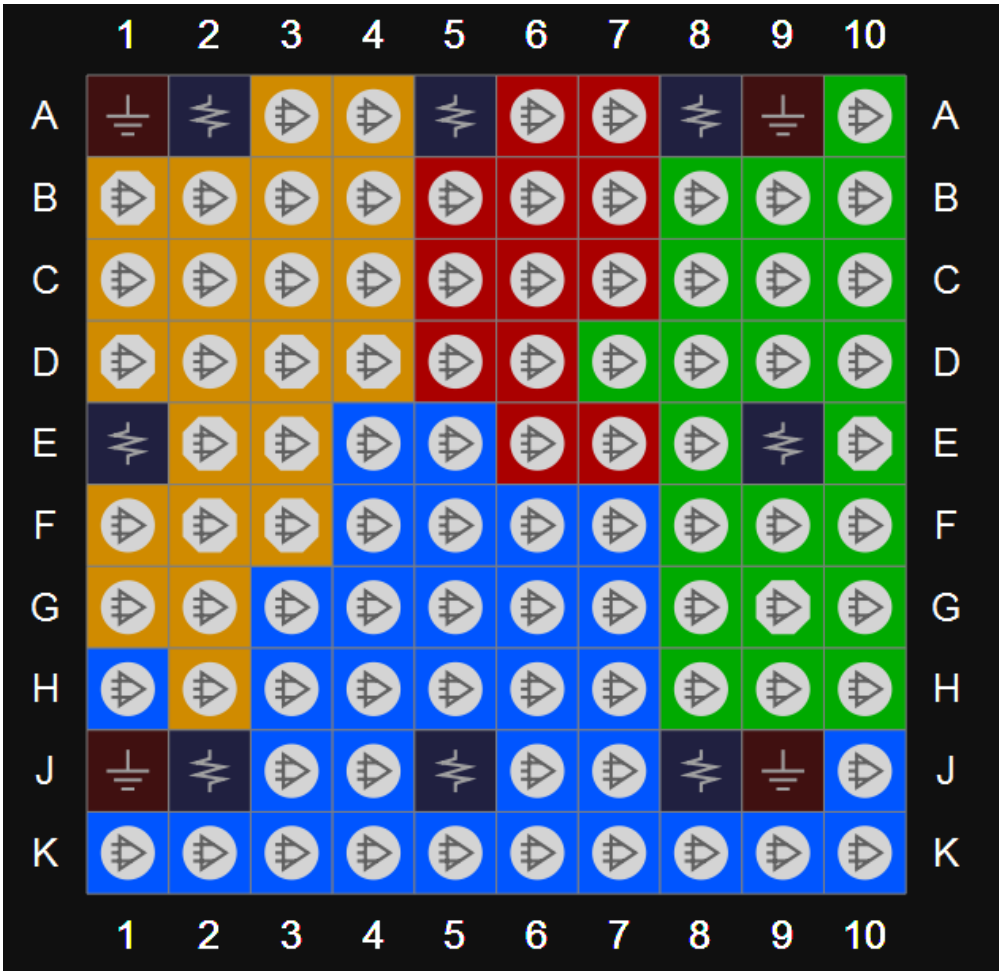



**Table 3-13 Other pins in GW1NR-9 MG100PF**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

## 3.4.5 View of LQ144P Pins Distribution

**Figure 3-14 View of GW1NR-9 LQ144P Pins Distribution (Top View)**


**Table 3-14 Other pins in GW1NR-9 LQ144P**

| | |
|---|---|
| VCC | 1, 36, 73, 108 |
| VCCO0 | 109, 127 |
| VCCO1 | 91, 103 |
| VCCO2 | 37, 55 |
| VCCO3 | 9, 19 |
| VCCX | 31, 77 |
| MODE | 143, 144 |
| VSS | 2, 17, 33, 35, 53, 74, 89, 105, 107 |

## 3.4.6 View of MG100PA Pins Distribution

**Figure 3-15 View of GW1NR-9 MG100PA Pins Distribution (Top View)**

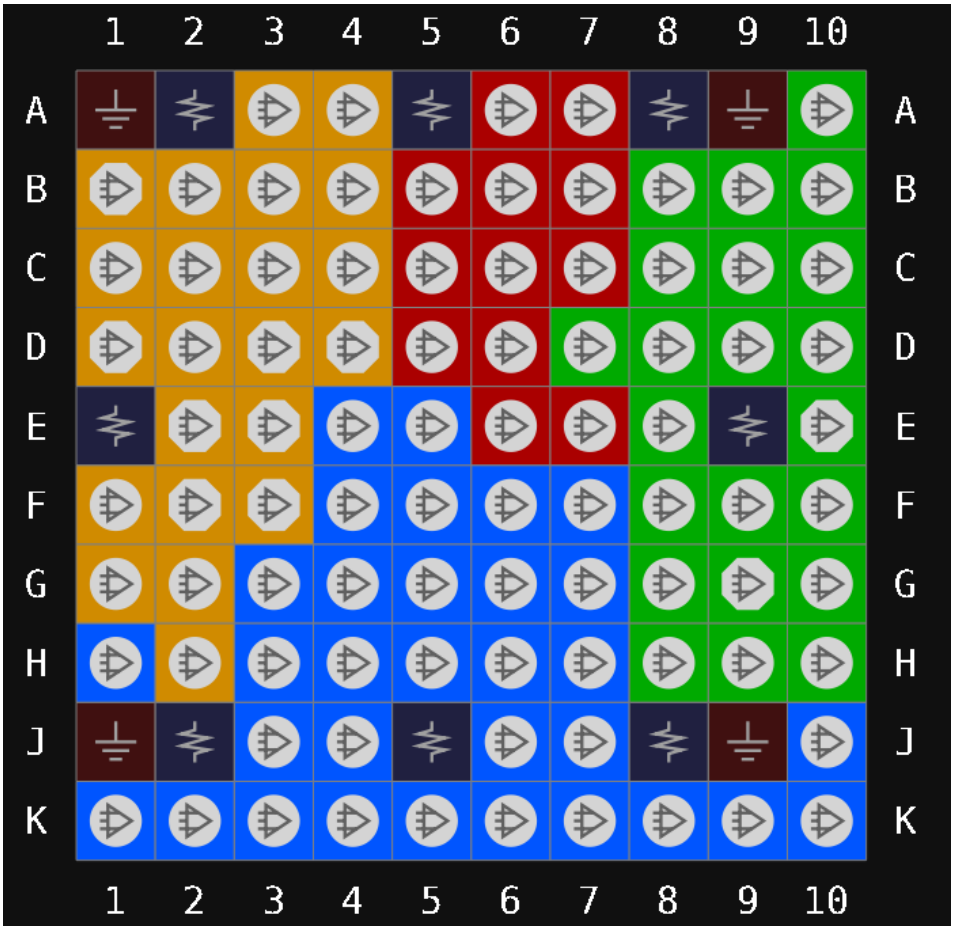



**Table 3-15 Other pins in GW1NR-9 MG100PA**

| | |
|---|---|
| VCC | A2,J2,A8 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

## 3.4.7 View of MG100PS Pins Distribution

**Figure 3-16 View of GW1NR-9 MG100PS Pins Distribution (Top View)**

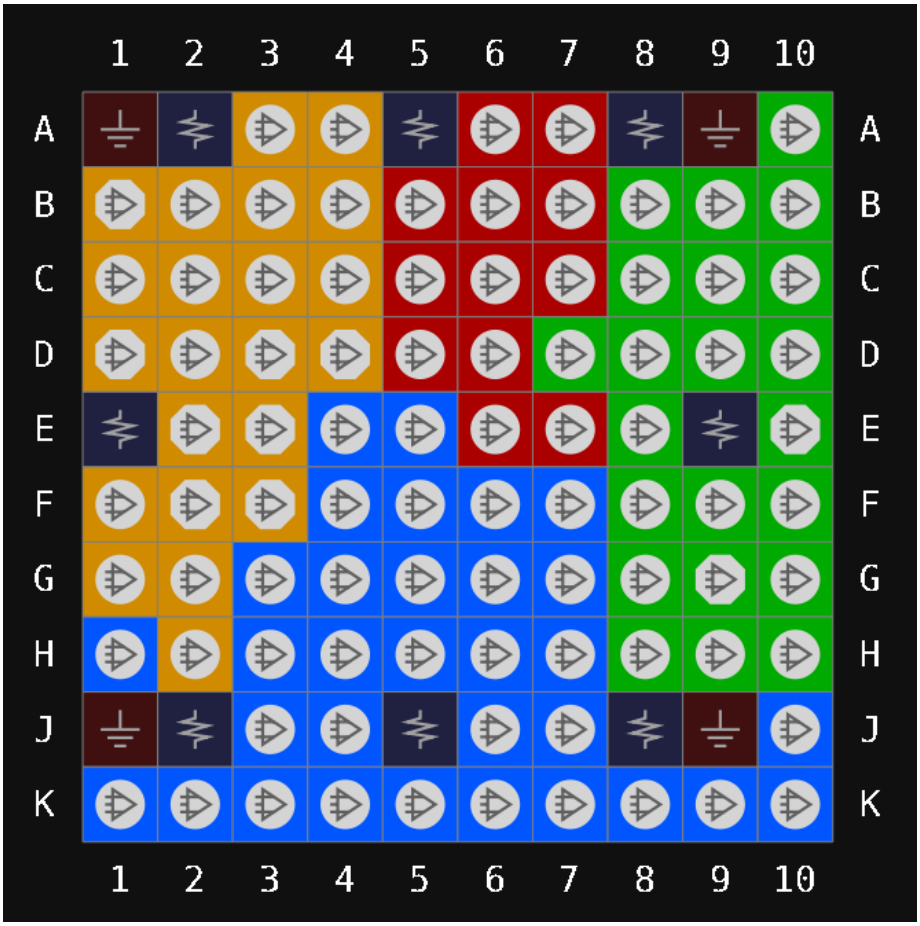



**Table 3-16 Other pins in GW1NR-9 MG100PS**

| | |
|---|---|
| VCC | A2,A8,J2 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

## 3.4.8 View of MG100PT Pins Distribution

**Figure 3-17 View of GW1NR-9 MG100PT Pins Distribution (Top View)**

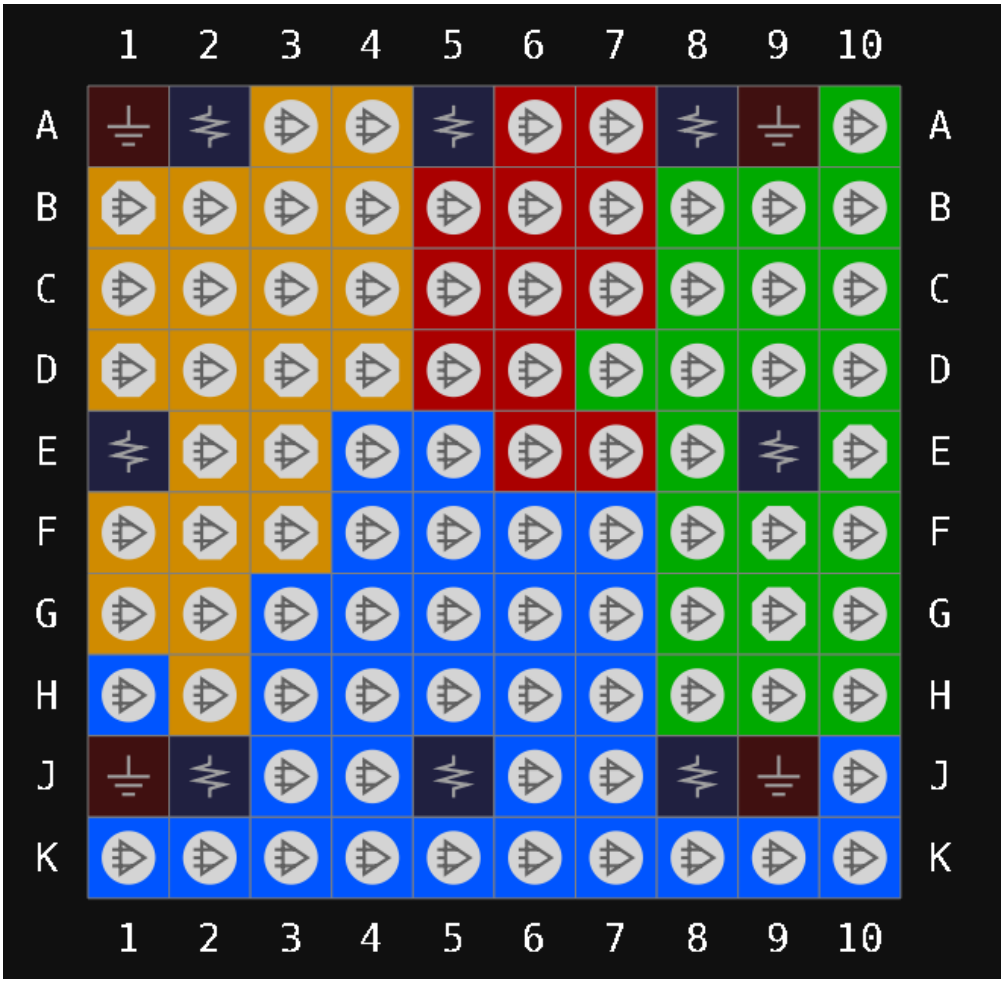


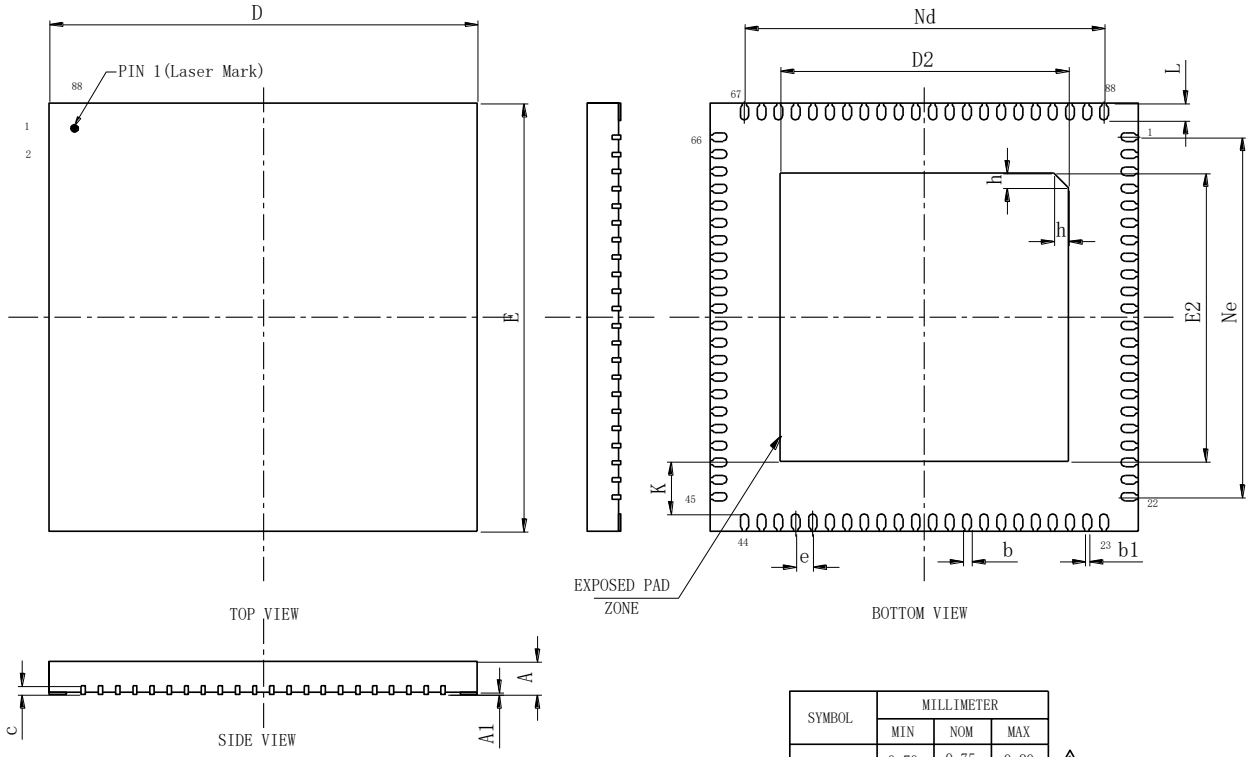

**Table 3-17 Other pins in GW1NR-9 MG100PT**

| | |
|---|---|
| VCC | A2,A8,J2 |
| VCCO0 | A5 |
| VCCO1 | E9 |
| VCCO2 | J5 |
| VCCO3 | E1 |
| VCCX | J8 |
| MODE | D4 |
| VSS | A1,A9,J1,J9 |

# 4 Package Diagrams

# 4.1 QN88/QN88P Package Outline (10mm x 10mm)

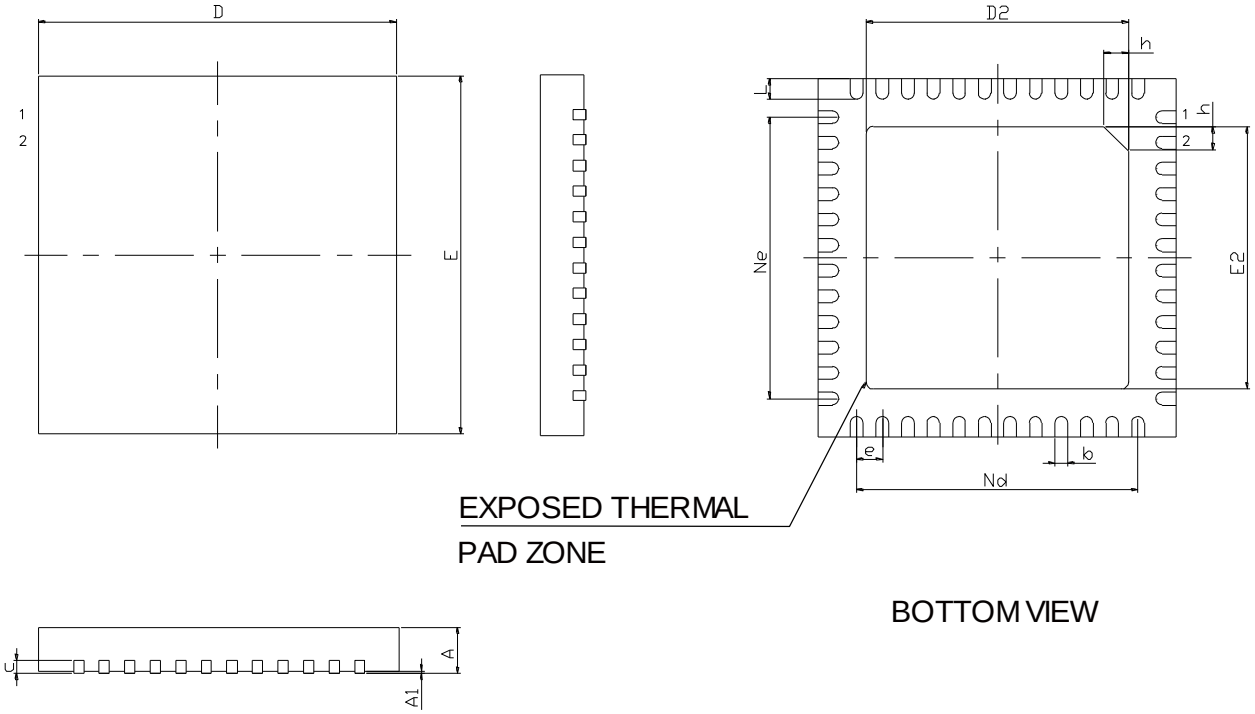
**Figure 4-1 Package Outline QN88/QN88P**




| SYMBOL | MILLIMETER | | | |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | 0.70 | 0.75 | 0.80 | ① |
| | 0.80 | 0.85 | 0.90 | |
| | 0.85 | 0.90 | 0.95 | ② |
| A1 | 0 | 0.02 | 0.05 | |
| b | 0.15 | 0.20 | 0.25 | |
| b1 | 0.10REF | | | ② |
| c | 0.18 | 0.20 | 0.25 | |
| D | 9.90 | 10.00 | 10.10 | |
| D2 | 6.64 | 6.74 | 6.84 | |
| e | 0.40BSC | | | |
| Nd | 8.40REF | | | |
| E | 9.90 | 10.00 | 10.10 | |
| E2 | 6.64 | 6.74 | 6.84 | |
| Ne | 8.40REF | | | |
| L | 0.30 | 0.40 | 0.50 | |
| K | 0.20 | – | – | |
| h | 0.30 | 0.35 | 0.40 | |
| L/F载体尺寸 (mil) | 300x300 | | | |

# 4.2 QN48G Package Outline (6mm x 6mm)

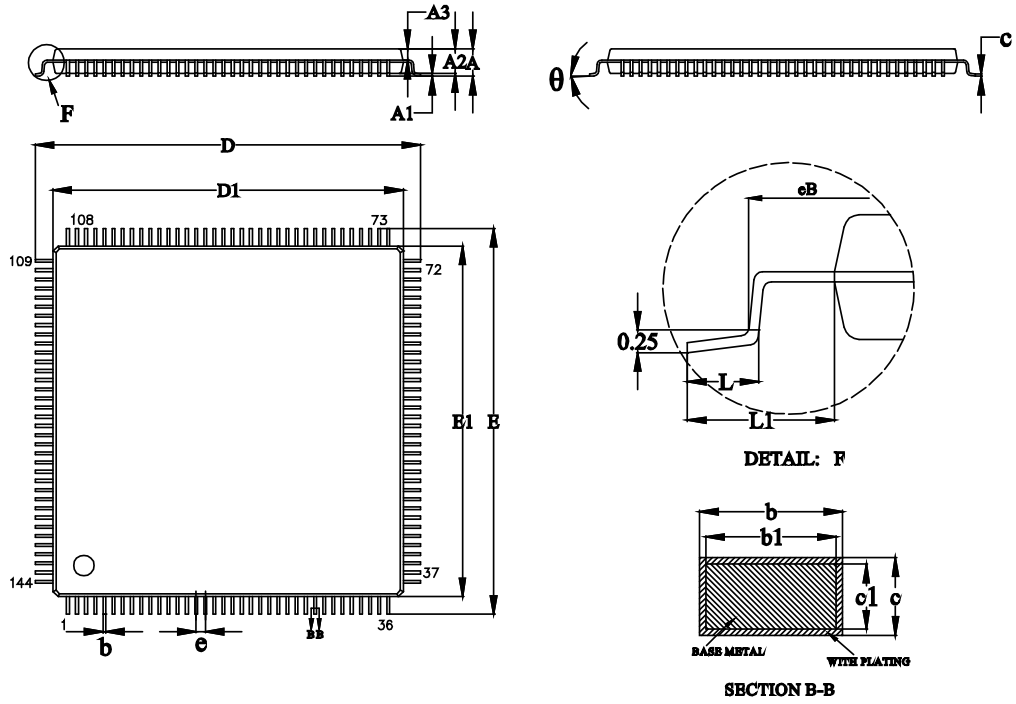
**Figure 4-2 Package Outline QN48G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.75 | 0.85 | 0.85 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.23 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 4.10 | 4.20 | 4.30 |
| e | 0.40BSC | | |
| Ne | 4.40BSC | | |
| Nd | 4.40BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.10 | 4.20 | 4.30 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 (MIL) | 177*177 | | |

# 4.3 LQ144/LQ144P Package Outline (20mm x 20mm)

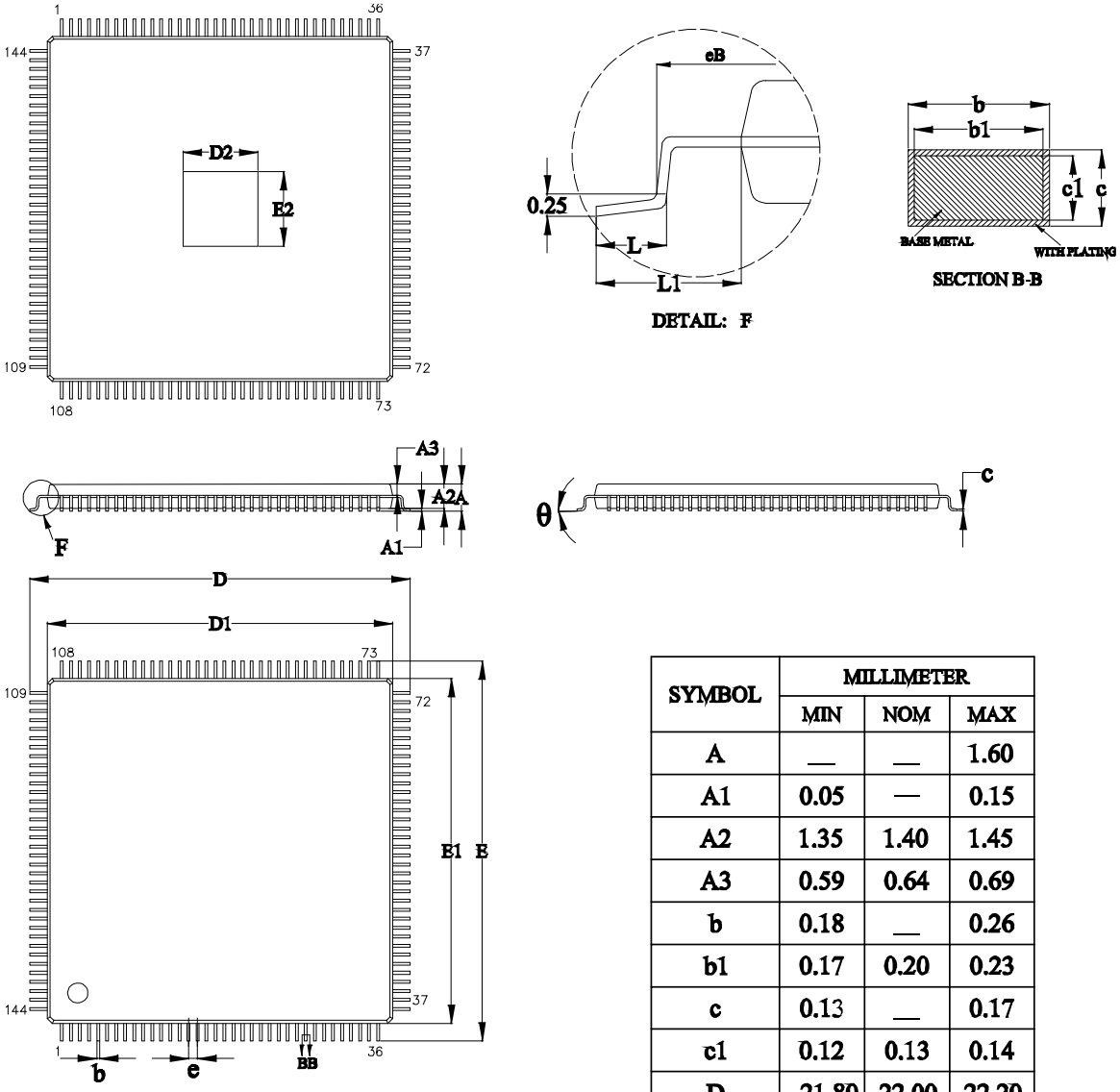
**Figure 4-3 Package Outline LQ144/LQ144P**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | 0.50BSC | | |
| L | 0.45 | — | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | — | 7° |

# 4.4 EQ144G Package Outline (20mm x 20mm)

**Figure 4-4 Package Outline EQ144G**

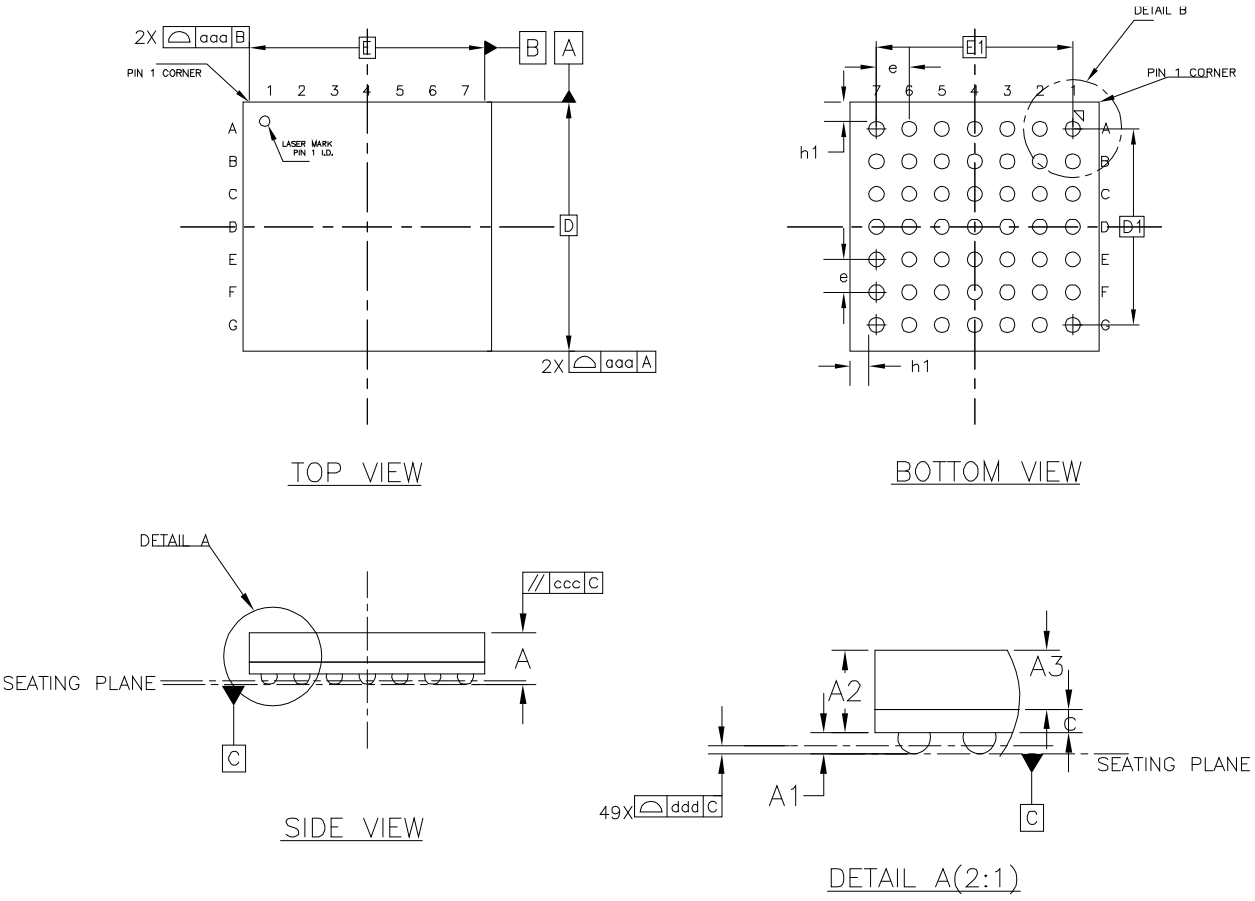



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | 0.50BSC | | |
| eB | 21.15 | | 21.40 |
| L | 0.45 | — | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | — | 7° |

| Size (mm) / Type (mil) | D2 | E2 |
|---|---|---|
| 218*218 | 5.00REF | 5.00REF |

# 4.5 MG49P/ MG49PG/MG49G Package Outline (3.8mm x 3.8mm)

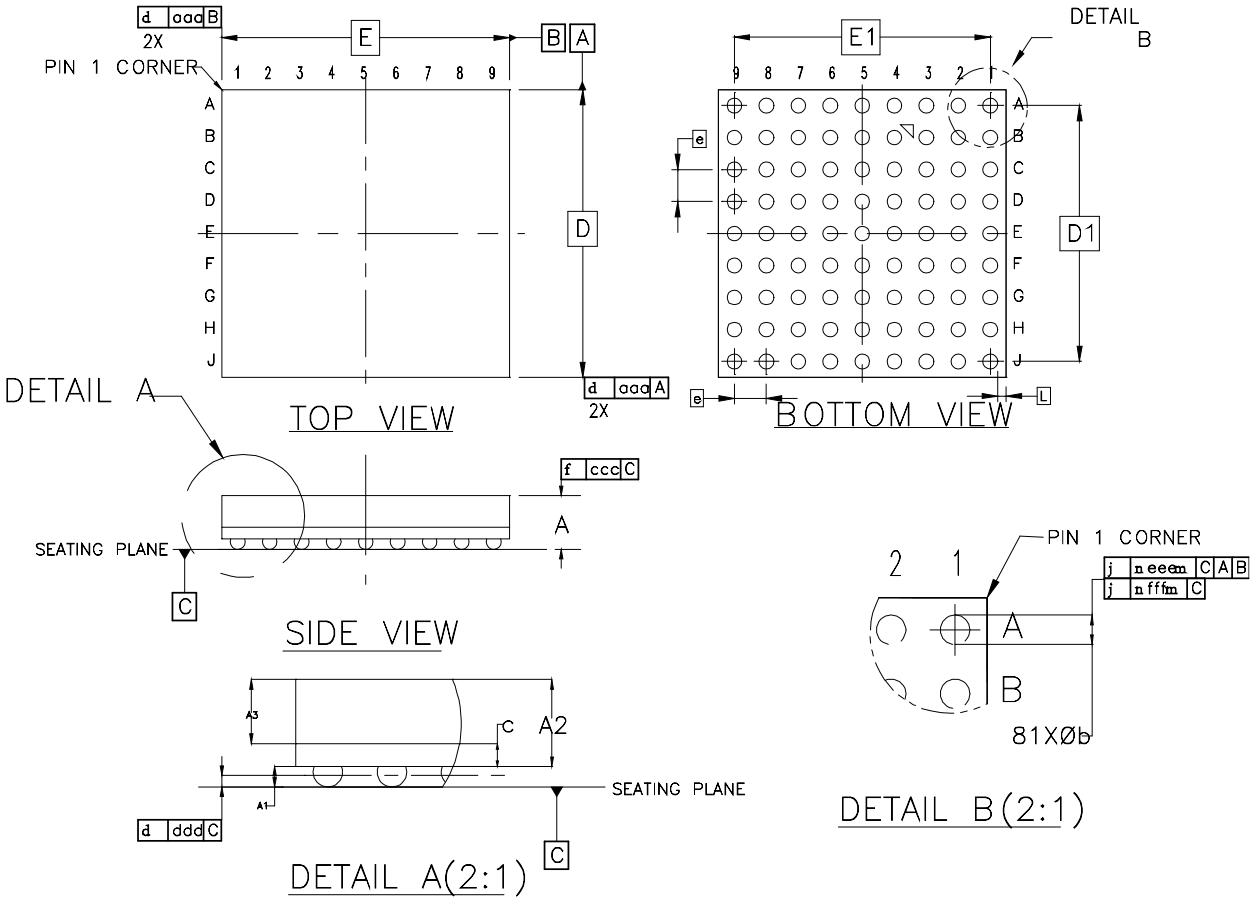
**Figure 4-5 Package Outline MG49P/ MG49PG/MG49G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.71 | 0.79 | 0.87 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.58 | 0.63 | 0.68 |
| A3 | | 0.45 BASIC | |
| c | 0.15 | 0.18 | 0.21 |
| D | 3.70 | 3.80 | 3.90 |
| D1 | | 3.00 BASIC | |
| E | 3.70 | 3.80 | 3.90 |
| E1 | | 3.00 BASIC | |
| e | | 0.50 BASIC | |
| b | 0.18 | 0.23 | 0.28 |
| h1 | | 0.285 REF | |
| aaa | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.08 | |
| eee | | 0.15 | |
| fff | | 0.05 | |

# 4.6 MG81P Package Outline (4.5mm x 4.5mm)

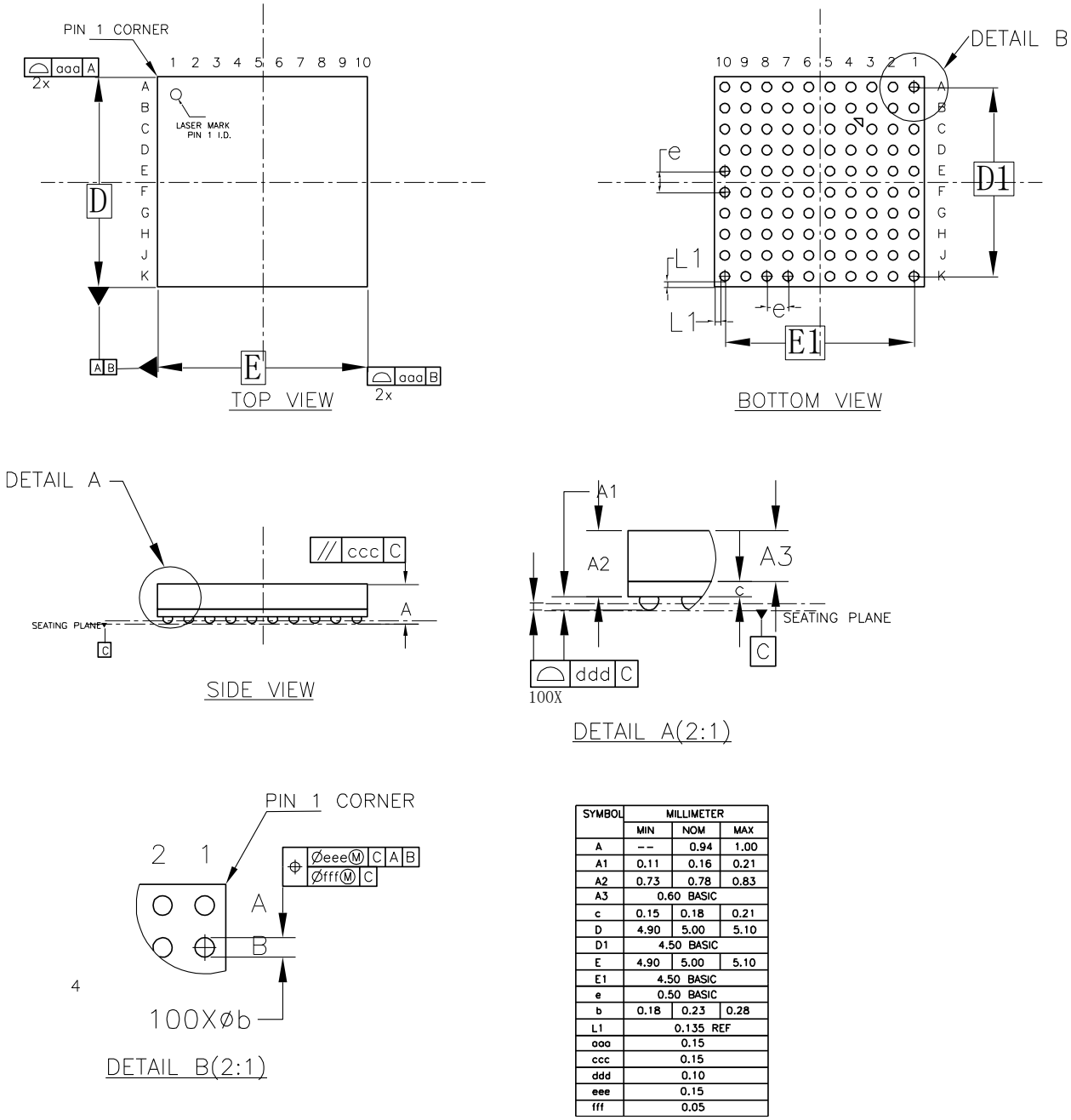
**Figure 4-6 Package Outline MG81P**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 0.84 | 0.90 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.63 | 0.68 | 0.73 |
| A3 | | 0.50 BASIC | |
| c | 0.15 | 0.18 | 0.21 |
| D | 4.40 | 4.50 | 4.60 |
| D1 | | 4.00 BASIC | |
| E | 4.40 | 4.50 | 4.60 |
| E1 | | 4.00 BASIC | |
| e | | 0.50 BASIC | |
| b | 0.18 | 0.23 | 0.28 |
| L | | 0.135 TYP | |
| aaa | | 0.10 | |
| ccc | | 0.15 | |
| ddd | | 0.10 | |
| eee | | 0.15 | |
| fff | | 0.05 | |

# 4.7 MG100P/MG100PF/MG100PA/MG100PT MG100PS Package Outline (5mm x 5mm)

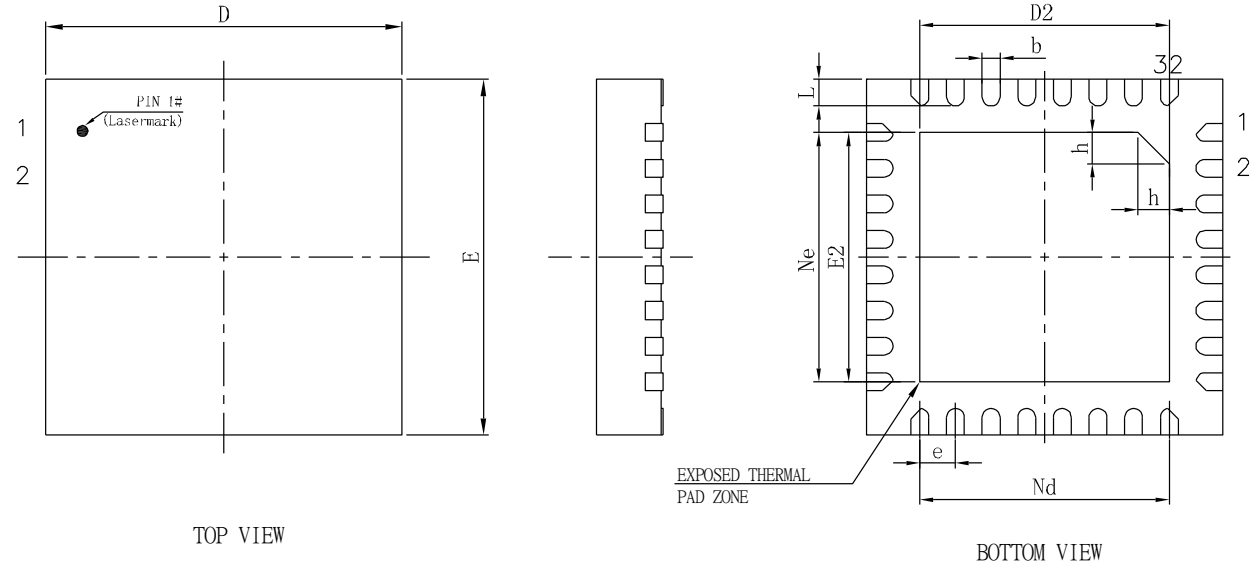
**Figure 4-7 Package Outline MG100P/MG100PF/MG100PA/ MG100PT**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 0.94 | 1.00 |
| A1 | 0.11 | 0.16 | 0.21 |
| A2 | 0.73 | 0.78 | 0.83 |
| A3 | 0.60 BASIC | | |
| c | 0.15 | 0.18 | 0.21 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 4.50 BASIC | | |
| E | 4.90 | 5.00 | 5.10 |
| E1 | 4.50 BASIC | | |
| e | 0.50 BASIC | | |
| b | 0.18 | 0.23 | 0.28 |
| L1 | 0.135 REF | | |
| aaa | 0.15 | | |
| ccc | 0.15 | | |
| ddd | 0.10 | | |
| eee | 0.15 | | |
| fff | 0.05 | | |

# 4.8 FN32G Package Outline (4mm x 4mm)

**Figure 4-8 Package Outline FN32G**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.70 | 2.80 | 2.90 |
| e | 0.40BSC | | |
| Ne | 2.80BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.70 | 2.80 | 2.90 |
| L | 0.25 | 0.30 | 0.35 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 | 122X122 | | |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