# GW1N/GW1NR Series of FPGA Products Schematic Manual

## Introduction

Users should follow a series of rules during circuit board design when using the GW1N series of FPGA products. This manual describes the characteristics and special features of the GW1N/GW1NR series of FPGA products and provides a comprehensive checklist to guide design processes. The main contents of this guide are as follows:

- Power Supply
- JTAG Download
- MSPI Download
- Clock Pin
- Difference Pin
- READY, RECONFIG_N, DONE
- MODE
- JTAGSEL_N
- FASTRD_N
- Pin Multiplex
- Reference for the External Crystal Oscillator Circuit
- GW1NR Bank Voltage
- Supported Configuration Modes
- Pin Distribution

## Power Supply

### Overview

The GW1N/GW1NR series of FPGA products support lower voltage (LV) and upper voltage (UV) with low power, instant on, and non-volatile power features. LV supports 1.2 V core voltages. UV supports 1.8 V, 2.5 V, and 3.3 V core voltages, and has a built-in linear voltage regulator. LV and UV have the same functions, and the pins are compatible.

Voltage types include core voltage ($V_{CC}$), auxiliary voltage ($V_{CCX}$) and bank voltage ($V_{CCIO}$).

$V_{CCX}$ is an auxiliary power supply that is used to connect the internal part of the chip, with a 2.5V or 3.3V power supply. If no $V_{CCX}$ exists, I/O, OSC, and BSRAM circuits will be impacted and the chip will not be

functional.

### Power Index

The core voltage, $V_{CC}$ and $V_{CCO3}$, are used for internal power-on reset/set in the GW1N/GW1NR series of FPGA products. $V_{CCO0}$ ~ $V_{CCO2}$ are used to power up the other I/O BANKs. The device will only operate normally if the power supply voltages reach the recommended working range.

Table 1 lists the recommended working range for each power voltage.

**Table 1 Recommended Working Range**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | LV: Core Power | 1.14V | 1.26V |
| | UV:Core Power | 1.71V | 3.465V |
| $V_{CCO}$ | I/O Bank Power for LV | 1.14V | 3.6V |
| | I/O Bank Power for UV | 1.14V | 3.465V |
| $V_{CCX}$ | LV: Auxiliary Power | 2.375V | 3.465V |
| | UV: Auxiliary Power | 2.375V | 3.465V |

### Total Power

For specific density, packages, and resource utilization, GPA tools can be used to evaluate and analyze the power consumption.

### Power-on time

Reference range of power-on time: 0.2ms ~2ms.

**Note!**

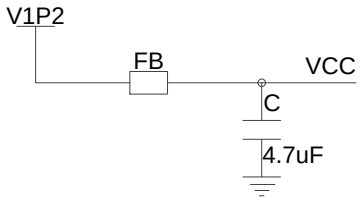
- If the power-on time is more than 2ms, you need to ensure that the power-on in sequence is $V_{CC}$, and then $V_{CCX}$/$V_{CCIO}$;
- If the power-on time is less than 0.2ms, it is recommended to increase the capacitance to prolong the power-on time.

### Power Filter

Each FPGA power input pin is connected to the ground with a 0.1uF ceramic capacitor.

The input end of the $V_{CC}$ core voltage should primarily conduct the noise processing. Specific reference is as shown in Figure 1:

**Figure 1 $V_{CC}$ Noise processing on the Input End of the Vcc Core Voltage**




FB is a magnetic bead, reference model mh2029-221y, ceramic

capacitance 4.7uF. It offers an accuracy of more than ±10%.

# JTAG Download

## Overview

JTAG download is used for downloading the bitstream data into the SRAM, on-chip flash or off-chip flash of the FPGA.

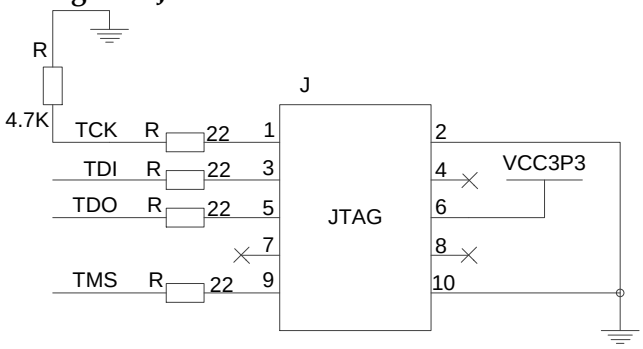
## Signal Definition

**Table 2 Signal Definition of JTAG Configuration Mode**

| Name | I/O | Description |
|---|---|---|
| TCK | I | Serial clock input in JTAG mode |
| TMS | I, internal weak pull-up | Serial mode input in JTAG mode |
| TDI | I, internal weak pull-up | Serial data input in JTAG mode |
| TDO | O | Serial data output in JTAG mode |

## JTAG Circuit Reference

**Figure 2 JTAG Circuit Reference**




**Note!**

- The resistance accuracy is not less than 5%;
- The power supply of the 6th pin in the JTAG socket can be adjusted to VCC1P2, VCC1P5, VCC1P8 and VCC2P5 as required.

# MSPI Download

## Overview

As a master device, the MSPI configuration mode reads the configuration data automatically from the off-chip flash and sends it to the FPGA SRAM.

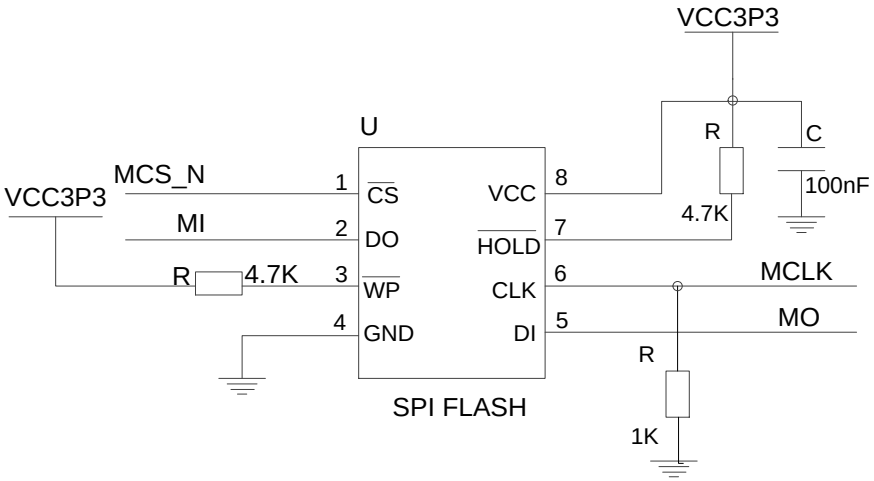
### Signal Definition

**Table 3 Signal Definition for MSPI Configuration Mode**

| Name | I/O | Description |
|---|---|---|
| MCLK | O | Clock output in MSPI mode |
| MCS_N | O | MCS_N in MSPI mode, low-active |
| MI | I | Data input in MSPI mode |
| MO | O | Data output in MSPI mode |

### MSPI Circuit Reference

**Figure 3 MSPI Circuit Reference**




**Note!**

- 1K pull-down resistance is required for MCLK signal.
- The resistance accuracy is not less than 5%.

# Clock Pin

### Overview

The clock pins include GCLK global clock pins and PLL clock pins.

- GCLK: The GCLK pins in the GW1N/GW1NR series of FPGA products distribute in the L and R quadrants. Each quadrant provides eight GCLK networks. The optional clock resources of the GCLK can be I/Os or CRU. Selecting the clock from the dedicated I/Os can result in better timing.
- PLL: Frequency (multiply and division), phase, and duty cycle can be adjusted by configuring the parameters.

### Signal Definition

**Table 4 Signal Definition for Clock Pin**

| Name | I/O | Description |
|---|---|---|
| GCLKT_[x] | I/O | Pins in global clock input, T(True), [x]: global clock No. |
| GCLKC_[x] | I/O | Pins for Global clock input, C(Comp), [x]: global |

| Name | I/O | Description |
|---|---|---|
| | | clock No. |
| LPLL_T_fb/RPLL_T_fb | I | L/R PLL feedback the input pin, T(True) |
| LPLL_C_fb/RPLL_C_fb | I | L/R PLL feedback the input pin, C(Comp) |
| LPLL_T_in/RPLL_T_in | I | L/R PLL clock input pin, T(True) |
| LPLL_C_in/RPLL_C_in | I | L/R PLL clock input pin, C(Comp) |

### Clock Input Selection

If the external clock inputs as a PLL clock, the user is advised to input from the PLL dedicated pin. And the PLL_T end is selected if the external clock inputs from the single-end.

GCLK is the global clock and is directly connected to all resources in the device. The GCLK_T end is advised if the GCLK inputs from the single-end.

# Differential Pin

### Overview

Differential transmission is a form of signal transmission technology that operates according to differences between the signal line and the ground line. The differential transmit signals on these two lines, the amplitude of the two signals are equal and have the same phase but demonstrate opposite polarity.

### LVDS

LVDS is a low-voltage differential signal that offers low power consumption, low bit error rate, low crosstalk, and low radiation. It facilitates the transmission of data using a low-voltage swing high-speed differential. Different packages employ different signals. Please refer to the True LVDS section of the Package Pinout Manual for further details.

**Notes**

- BANK1/2/3 in the GW1N/GW1NR series of FPGA products support true LVDS output. BANK0 in the GW1N/GW1NR series of FPGA products supports 100 Ω input differential matched resistance;
- If BANK 1/2/3 are used as the differential input, 100-ohm terminal resistance is needed;
- The different line impedance of PCB is controlled at about 100 ohms.

# READY, RECONFIG_N, DONE

### Overview

RECONFIG_N is a reset function within the FPGA programming configuration. FPGA can't configure if RECONFIG_N is low.

As a configuration pin, a low level signal with pulse width no less than 25ns is required to start GowinCONFIG to reload bitstream data according

to the MODE setting value. You can control the pin via the write logic and trigger the device to reconfigure.

READY, the FPGA can configure only when the READY signal is high. The device should be restored by using the power on or triggering RECONFIG_N when the READY signal is low.

As an output configuration pin, FPGA can be indicated for the current configuration state. If the device meets the configuration condition, READY signal is high. If the device fails to configure, the READY signal changes to low. As an input configuration pin, you can reduce the READY signal via its own logic or manually operate outside the device to delay configuration.

DONE, the DONE signal indicates that the FPGA is configured successfully. The signal is high after successful configuration.

As an output configuration pin, FPGA can be indicated whether the current configuration is successful. If configured successfully, DONE is high, and the device enters into a working state. If the device failed to configure, the DONE signal remains low. For the input type, the user can reduce the READY signal via its own internal logic or manually operate outside the device to delay progression to user mode.

When the RECONFIG_N or READY signals are low, the DONE signal is low. DONE has no influence when SRAM is configuried through the JTAG circuit.

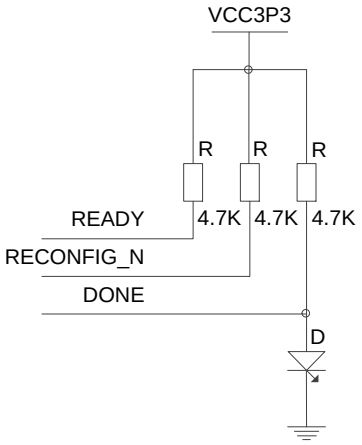
### Signal Definition

**Table 5 READY, RECONFIG_N, DONE Signal Definition**

| Name | I/O | Description |
|---|---|---|
| RECONFIG_N | I, internal weak pull-up | Low level pulse: start new GowinCONFIG configuration |
| READY | I/O | High-level pulse: The device can currently be programmed and configured; |
| | | Low-level pulse: The device cannot be programmed and configured, |
| DONE | I/O | High-level pulse: The device has been successfully programmed and configured; |
| | | Low-level pulse: The configuration is incomplete or has failed. |

### READY, RECONFIG_N, DONE Reference Circuit

**Figure 4 READY, RECONFIG_N, DONE Reference Circuit**




**Note!**

- The upper pull power supply is the bank voltage value of the corresponding pin;
- The resistance accuracy is not less than ± 5%.

# MODE

## Overview

MODE spans the MODE0, MODE1, MODE2, and GowinCONFIG configuration modes. When the FPGA powers on or a low pulse triggers the RECONFIG_N mode, the device enters the corresponding GowinCONFIG state according to the MODE value. As the number of pins for each package is different, some MODE pins are not all packaged, and the unpacked MODE pins are grounded inside. Please refer to the corresponding PINOUT manual for further details.

## Signal Definition

**Table 6 MODE Signal Definition**

| Name | I/O | Description |
|---|---|---|
| MODE2 | I, internal weak pull-up | GowinCONFIG modes selection pin. |
| MODE1 | I, internal weak pull-up | GowinCONFIG modes selection pin. |
| MODE0 | I, internal weak pull-up | GowinCONFIG modes selection pin. |

## Mode Selection

**Table 7 Mode Selection**

| Configuration | | MODE[2:0] | Instructions |
|---|---|---|---|
| JTAG | | XXX | The GW1N series of FPGA products are configured by hardware processor via a JTAG interface. |
| GowinCONFIG | AUTO BOOT | 000 | The GW1N series of FPGA products are configured by reading data from built-in flash. |

| | | | |
|---|---|---|---|
| | SSPI | 001 | The GW1N series of FPGA products are configured by hardware processor via an SPI interface. |
| | MSPI | 010 | As master, the GW1N series of FPGA products are configured by reading data from an external flash (or alternative device) through an SPI interface. |
| | DUAL BOOT | 100 | Reads from built-in flash first and then from external flash if the built-in flash configuration fails. |
| | SERIAL | 101 | The GW1N series of FPGA products are configured by hardware processor via a DIN interface. |
| | CPU | 111 | The GW1N series of FPGA products are configured by hardware processor via a DBUS interface. |

# JTAGSEL_N

## Overview

Select the signal in JTAG mode. If the JTAG pin is set as GPIO in Gowin software, the JTAG pin is changed to GPIO pin after being powered on and successfully configured. The JTAG pin can be recovered by reducing the JTAGSEL_N. The JTAG configuration functions are always available if no JTAG pin multiplexing is set.

## Signal Definition

**Table 8 JTAGSEL_N Signal Definition**

| Pin Name | I/O | Description |
|---|---|---|
| JTAGSEL_N | I, internal weak pull-up | Restore JTAG pin from GPIO to configuration pin. Low level is valid |

**Note!**

As GPIO, the JTAGSEL_N pin and four pins (TCK, TMS, TDI, and TDO) configured with JTAG are incompatible: the JTAG pin can only be used as a configuration pin if JTAGSEL_N is set as GPIO. JTAGSEL_N can only be used as a configuration pin if JTAG is set as GPIO.

# FASTRD_N

## Overview

In MSPI configuration mode, signals are selected via reading the SPI flash speed rate. FASTRD_N is normal read mode if it is high level; FASTRD_N is high speed read mode if it is low level. Each manufacturer's Flash high speed read instruction is different; please refer to the corresponding Flash data manual.

### Signal Definition

**Table 9 FASTRD_N Signal Definition**

| Pin Name | I/O | Description |
|---|---|---|
| FASTRD_N | I/O | ● As a configuration pin: Input, internal weak pull up, sample MSPI configuration value at READY signal rising edge;<br>● As a GPIO: Input or putput. |

**Note!**

- High-level: Normal Flash access mode, the clock frequency should be less than 30MHz;
- Low-level: High-speed Flash access mode, the clock frequency is greater than 30MHz and less than 80MHz.

# Pin Multiplexing

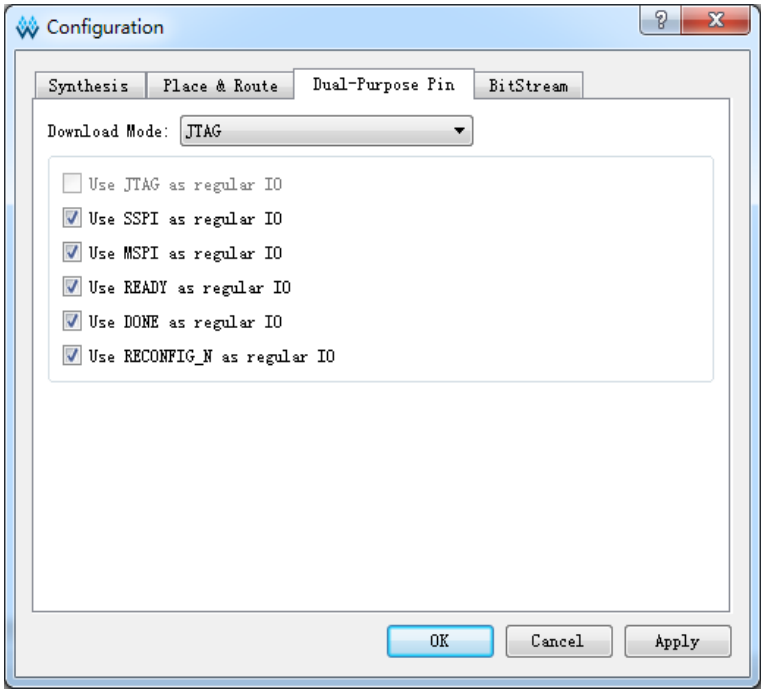
### Overview

Configure pin multiplexing refers to configuring during power-on, which is used as a normal I/O after downloading the bitstream file.

Configure pin multiplex via the Gowin software:

a). Open the corresponding project in Gowin software;
b). Select “Project > Configuration > Dual Purpose Pin” from the menu options, as shown in Figure 5;
c). Check the corresponding option to set the pin multiplex.

**Figure 5 Pin Multiplex**




### Pin Multiplex

- SSPI: As a GPIO, SSPI can be used as input or output type;
- MSPI: As a GPIO, MSPI can be used as input or output type;
- RECONFIG_N GPIO can only be used as an output type. For smooth

configuration, set the initial value of RECONFIG_N as high when multiplexing it.

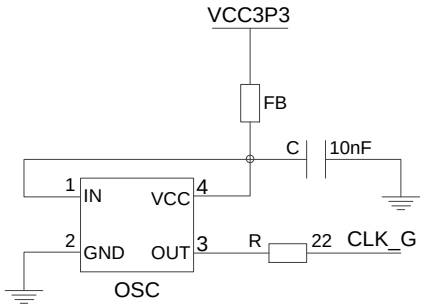
- READY: As a GPIO, READY can be used as an input or output. As an input GPIO for READY, the initial value of READY should be 1 before configuring. Otherwise, the FPGA will fail to configure;
- DONE: As a GPIO, DONE can be used as an input or output type. If DONE is used as an input GPIO, the initial value of DONE should be 1 before configuring. Otherwise, the FPGA will fail to enter the user mode after configuring;
- JTAG: As a GPIO, JTAG can be used as an input or output type;
- JTAGSEL_N: As a GPIO, JTAGSEL_N can be used as an input or output type.
- DONE: as a GPIO, DONE can be used as an input or output type. In order to smoothly configure, the user multiplexes the MODE pin, the correct configuration mode value is needed to provided during configuration (power-on or low-level pulse triggers RECONFIG_N). Three pins can be multiplexed in the MODE. Unpackaged devices are grounded internally. Please refer to PINOUT manual of the corresponding device for details. For the MODE value corresponding to different configuration modes, please refer to the corresponding device configuration and programming manual

**Note!**

If the Number of I/O port is sufficient, use non-multiplexed pins first.

# FPGA External Crystal Oscillator Circuit Reference

**Figure 6 FPGA External Crystal Oscillator Circuit Reference**




FB is a magnetic bead, with MH2029-221Y reference model, more than ±5% resistance accuracy, and more than ±10% capacitance accuracy.

# Bank Voltage

For the detailed Bank voltage requirements, please refer to the following manuals.

- UG107, GW1N-1 Pinout
- UG105-1.3, GW1N-2&2B&4&4B Pinout
- UG114-1.08, GW1N-6&9 Pinout
- UG167-1.0, GW1N-1S Pinout
- UG116-1.06, GW1NR-4&4B Pinout
- UG801-1.4, GW1NR-9 Pinout

# Supported Configuration Modes

## GW1N-1 Configuration Modes

**Table 10 GW1N-1 Configuration Modes**

| Configuration Mode | JTAG | AUTO BOOT | SSPI | MSPI | DUAL BOOT | SERIAL | CPU |
|---|---|---|---|---|---|---|---|
| CS30 | √ | √ | √ | -- | -- | -- | -- |
| QN32 | √ | √ | √ | -- | -- | -- | -- |
| QN48 | √ | √ | √ | √ | -- | -- | -- |
| LQ100 | √ | √ | √ | -- | -- | -- | -- |
| LQ144 | √ | √ | √ | √ | -- | -- | -- |
| MG160 | √ | √ | √ | √ | √ | √ | √ |
| PG204 | √ | √ | √ | √ | √ | √ | √ |

## GW1N-4 Configuration Modes

**Table 11 GW1N-4 Configuration Modes**

| Configuration Mode | JTAG | AUTO BOOT | SSPI | MSPI | DUAL BOOT | SERIAL | CPU |
|---|---|---|---|---|---|---|---|
| QN32 | √ | √ | -- | √ | -- | -- | -- |
| QN48 | √ | √ | -- | √ | -- | -- | -- |
| CS72 | √ | √ | √ | -- | -- | -- | -- |
| QN88 | √ | √ | -- | √ | -- | -- | -- |
| LQ100 | √ | √ | √ | -- | -- | -- | -- |
| LQ144 | √ | √ | √ | √ | -- | -- | -- |
| MG160 | √ | √ | √ | √ | √ | √ | √ |
| PG256 | √ | √ | √ | √ | √ | √ | √ |

## GW1N-9 Configuration Modes

**Table 12 GW1N-9 Configuration Modes**

| Configuration Mode | JTAG | AUTO BOOT | SSPI | MSPI | DUAL BOOT | SERIAL | CPU |
|---|---|---|---|---|---|---|---|
| QN48 | √ | √ | -- | -- | -- | -- | -- |
| QN88 | √ | √ | -- | √ | -- | -- | -- |
| LQ100 | √ | √ | √ | -- | -- | -- | -- |
| LQ144 | √ | √ | √ | √ | -- | -- | -- |
| MG160 | √ | √ | √ | √ | √ | √ | √ |
| LQ176 | √ | √ | √ | √ | √ | √ | √ |
| PG256 | √ | √ | √ | √ | √ | √ | √ |
| UG332 | √ | √ | √ | √ | √ | √ | √ |

### GW1NR-4 Configuration Modes

**Table 13 GW1NR-4 Configuration Modes**

| Configuration Mode | JTAG | AUTO BOOT | SSPI | MSPI | DUAL BOOT | SERIAL | CPU |
|---|---|---|---|---|---|---|---|
| QN88 | √ | √ | -- | √ | -- | -- | -- |

### GW1NR-9 Configuration Modes

**Table 14 GW1NR-9 Configuration Modes**

| Configuration Mode | JTAG | AUTO BOOT | SSPI | MSPI | DUAL BOOT | SERIAL | CPU |
|---|---|---|---|---|---|---|---|
| QN88 | √ | √ | -- | √ | -- | -- | -- |
| LQ144 | √ | √ | √ | √ | -- | -- | -- |

# Pin Distribution

Before designing circuits, users should take the overall FPGA pin distribution needs into consideration and make informed decisions related to the application of the device architecture features, including I/O LOGIC, global clock resources, PLL resources, etc.

GW1N (besides GW1N-1)/GW1NR bank1/2/3 support true LVDS output. When using true LVDS output, $V_{CCO}$ should be configured to 2.5 V or 3.3 V. Refer to *GW1N/GW1NR FPGA Product Pinout* to ensure that the corresponding pins support true LVDS output.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source ($V_{REF}$) as the reference voltage. Users can choose $V_{REF}$ from the internal reference voltage of the bank (0.5 x VCCO) or external reference voltage $V_{REF}$ using any I/O from the bank.

**Note!**

The device I/Os (except TCK) are all internal weak pull-up. After configuration, I/Os status is determined by user programs and constraints.

# Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: 00 86 0755 82620391

# Revision History

| Date | Version | Description |
|---|---|---|
| 12/13/2016 | 1.0E | Initial version. |
| 01/02/2018 | 1.1E | Related content added as follows:<br>● Pin Multiplexing;<br>● FPGA external crystal oscillator circuit reference;<br>● GW1NR bank voltage;<br>● Configuration modes supported by each device. |
| 04/23/2018 | 1.2E | Modify the power-on time reference range as “0.2ms~2ms” and add the remark information. |
| 06/29/2018 | 1.3E | Revise the schematic diagram style uniformly. |
| 04/03/2019 | 1.4E | The description of FASTRD_N updated. |
| 04/12/2019 | 1.5E | The description added: The device I/Os (except TCK) are all internal weak pull-up. |
| 05/10/2019 | 1.6E | Pull-down resistance for MCLK signal added. |
| 06/04/2019 | 1.7E | Bank Voltage description updated. |
| 11/26/2019 | 1.8E | The value described in Table 1 Recommended Working Range fixed. |

**Disclaimer**