

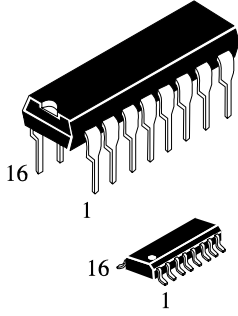
IN74HC138A

1-of-8 Decoder/Demultiplexer

The IN74HC138A is identical in pinout to the LS/ALS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

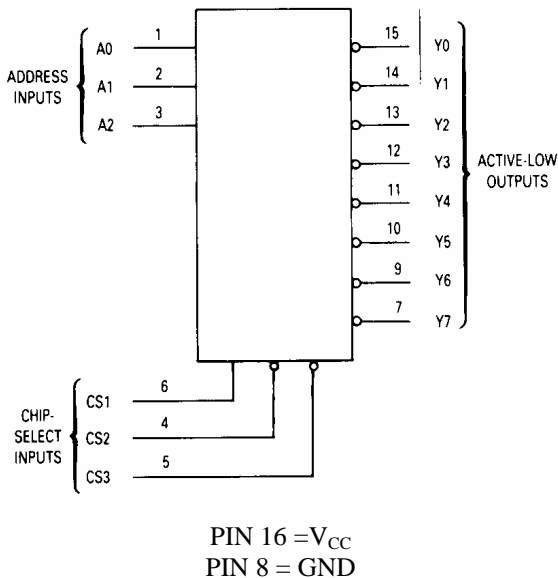


N SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION
 IN74HC138AN Plastic
 IN74HC138AD SOIC
 IZ74HC138A Chip
 T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT

A0	1	16	V _{CC}
A1	2	15	Y0
A2	3	14	Y1
CS2	4	13	Y2
CS3	5	12	Y3
CS1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

FUNCTION TABLE

Inputs				Outputs							
CS1	CS2	CS3	A2 A1 A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X X X	H	H	H	H	H	H	H	H
X	H	X	X X X	H	H	H	H	H	H	H	H
L	X	X	X X X	H	H	H	H	H	H	H	H
H	L	L	L L L	L	H	H	H	H	H	H	H
H	L	L	L L H	H	L	H	H	H	H	H	H
H	L	L	L H L	H	H	L	H	H	H	H	H
H	L	L	L H H	H	H	H	L	H	H	H	H
H	L	L	H L L	H	H	H	H	L	H	H	H
H	L	L	H L H	H	H	H	H	H	L	H	H
H	L	L	H H L	H	H	H	H	H	H	L	H
H	L	L	H H H	H	H	H	H	H	H	H	L

H = high level (steady state)
 L = low level (steady state)
 X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	V _{CC} = 2.0 V	0	1000	
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
t _{PLH} , t _{PHL}	Maximum Propagation Delay , CS1 to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t _{PLH} , t _{PHL}	Maximum Propagation Delay , CS2 or CS3 to Output Y (Figures 3 and 4)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Package)	Typical @25°C, V _{CC} =5.0 V				pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	55				

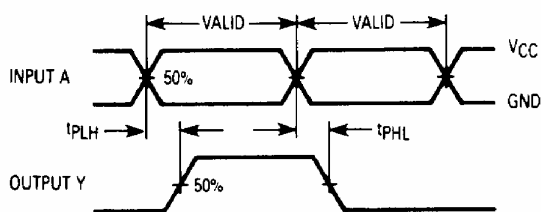


Figure 1. Switching Waveforms

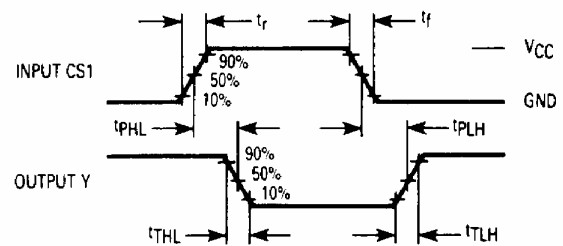


Figure 2. Switching Waveforms

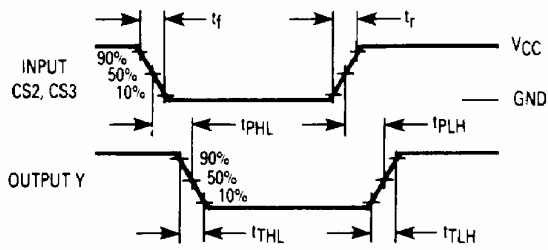
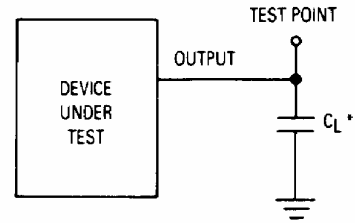


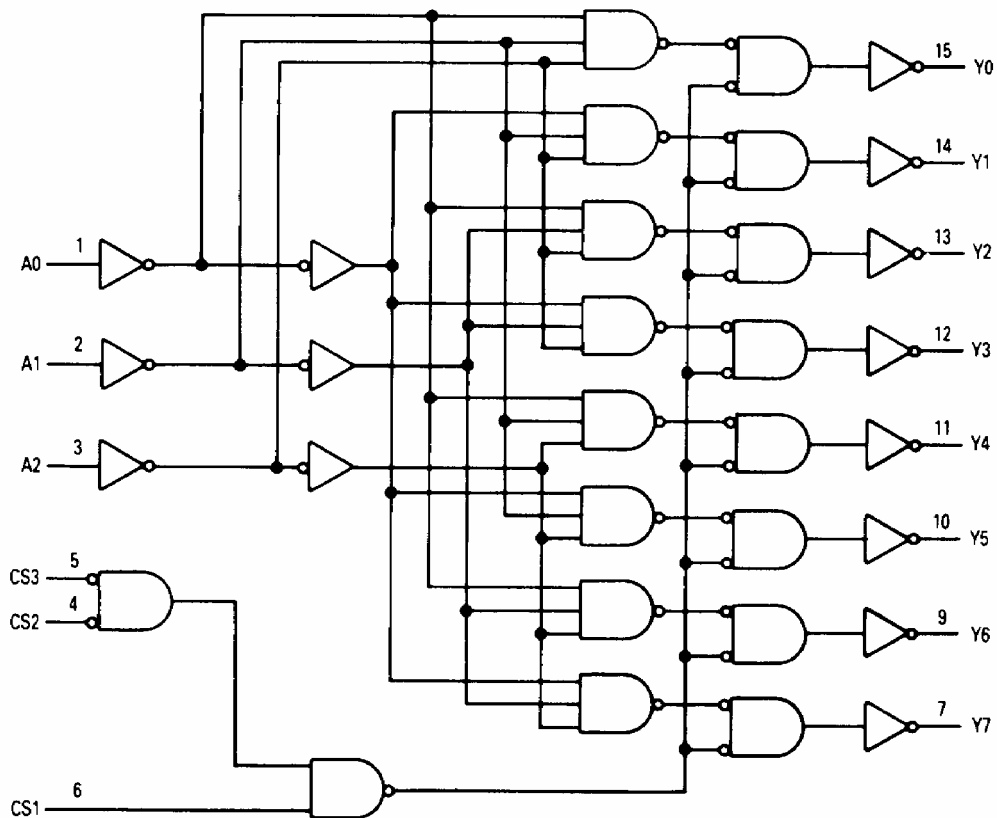
Figure 3. Switching Waveforms



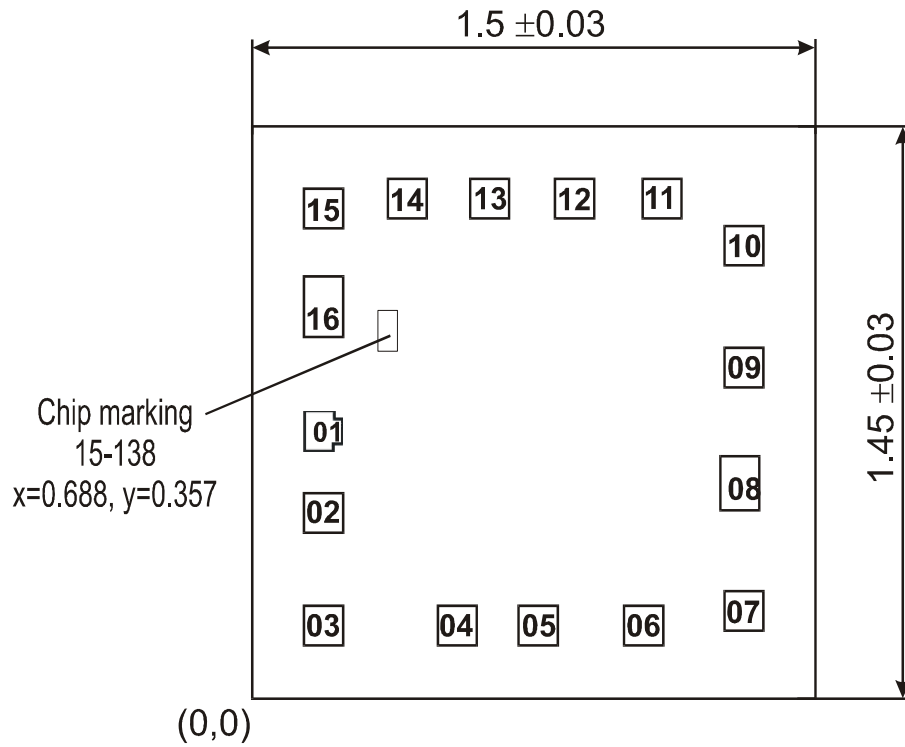
*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM IZ74HC138A



Pad size is given as per passivation layer
Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y	Pad size
01	SELECT a	0.161	0.690	0.106x0.106
02	A0a	0.161	0.360	0.106x0.106
03	A1a	0.150	0.165	0.106x0.106
04	Y0a	0.497	0.165	0.106x0.106
05	Y1a	0.661	0.165	0.106x0.106
06	Y2a	0.990	0.165	0.106x0.106
07	Y3a	1.261	0.196	0.106x0.106
08	GND	1.261	0.510	0.106x0.113
09	Y0b	1.260	0.793	0.106x0.106
10	Y1b	1.260	1.133	0.106x0.106
11	Y0b	1.034	1.202	0.106x0.106
12	Y1b	0.850	1.202	0.106x0.106
13	A2b	0.665	1.202	0.106x0.106
14	A3b	0.481	1.202	0.106x0.106
15	SELECT b	0.162	1.172	0.106x0.106
16	Vcc	0.170	0.863	0.106x0.113