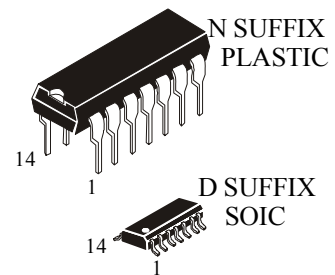


## IW4011B

### Quad 2-Input NAND Gate High-Voltage Silicon-Gate CMOS

The IW4011B NAND gates provide the system designer with direct implementation of the NAND function.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply



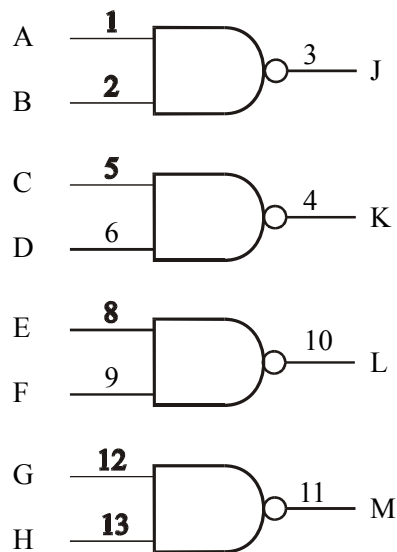
#### ORDERING INFORMATION

IW4011BN Plastic

IW4011BD SOIC

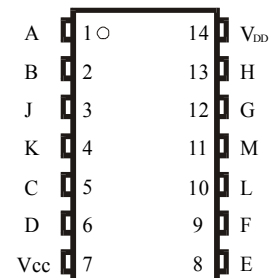
$T_A = -55^\circ$  to  $125^\circ$  C for all packages

#### LOGIC DIAGRAM



PIN 14 =  $V_{DD}$   
PIN 7 =  $V_{CC}$

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output
A	B	$J = A \cdot B$
C	D	$K = \overline{C \cdot D}$
E	F	$L = \overline{E \cdot F}$
G	H	$M = \overline{G \cdot H}$
H	H	L
H	L	H
L	H	H
L	L	H

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+	750	mW
	SOIC Package+	500	
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

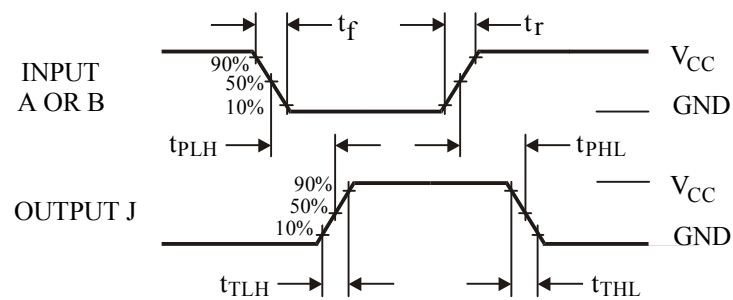
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V	5.0	3.5	3.5	3.5	V
		V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V	10	7	7	7	
		V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	15	11	11	11	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> = V <sub>CC</sub> - 0.5V	5.0	1.5	1.5	1.5	V
		V <sub>OUT</sub> = V <sub>CC</sub> - 1.0 V	10	3	3	3	
		V <sub>OUT</sub> = V <sub>CC</sub> - 1.5V	15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	0.25	0.25	7.5	μA
			10	0.5	0.5	15	
			15	1.0	1.0	30	
			20	5.0	5.0	150	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA
		U <sub>OL</sub> =0.4 V	5.0	0.64	0.51	0.36	
		U <sub>OL</sub> =0.5 V	10	1.6	1.3	0.9	
	U <sub>OL</sub> =1.5 V	15	4.2	3.4	2.4		
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA
		U <sub>OH</sub> =2.5 V	5.0	-2.0	-1.6	-1.15	
		U <sub>OH</sub> =4.6 V	5.0	-0.64	-0.51	-0.36	
		U <sub>OH</sub> =9.5 V	10	-1.6	-1.3	-0.9	
	U <sub>OH</sub> =13.5 V	15	-4.2	-3.4	-2.4		

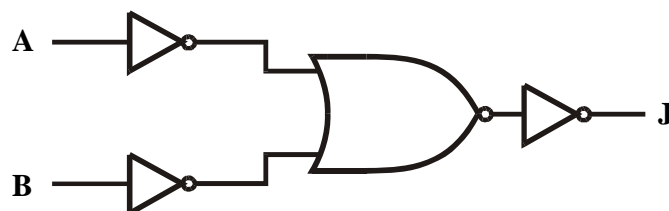
**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ ,  $R_L=200\text{k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figure 1)	5.0	250	250	250	ns
		10	120	120	120	
		15	90	90	90	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	200	ns
		10	100	100	100	
		15	80	80	80	
$C_{IN}$	Maximum Input Capacitance	-		7.5		pF

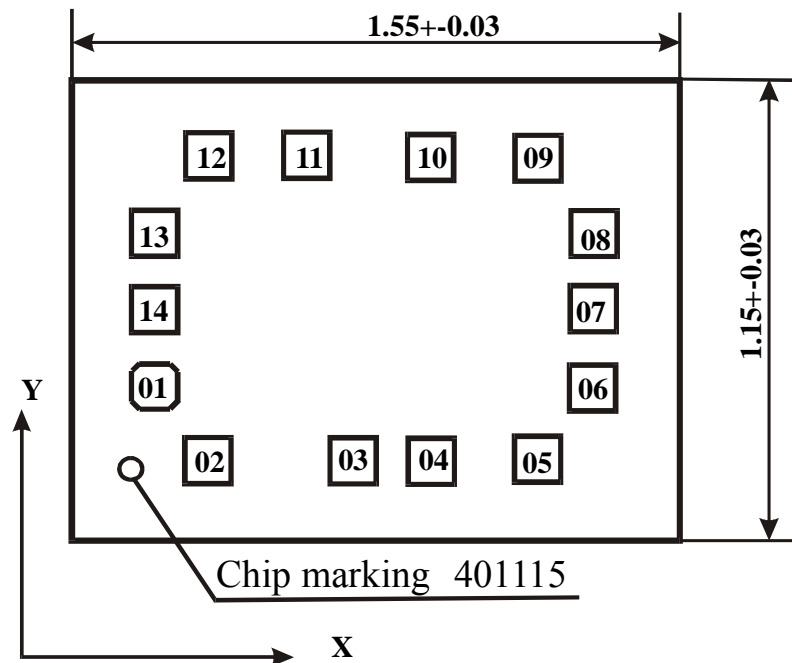


**Figure 1. Switching Waveforms**

**EXPANDED LOGIC DIAGRAM  
(1/4 of the Device)**



## CHIP PAD DIAGRAM



**Location of marking (mm):** left lower corner  $x = 0.095$ ,  $y = 0.100$ ;

**Thickness of chip:**  $0.46 \pm 0.02$  mm

## PAD LOCATION

Pad No.	Pad Name	X	Y	Pad size (mm)
01	A	0.111	0.306	0.120×0.120
02	B	0.253	0.110	0.120×0.120
03	J	0.615	0.110	0.120×0.120
04	K	0.815	0.110	0.120×0.120
05	C	1.176	0.110	0.120×0.120
06	D	1.315	0.306	0.120×0.120
07	V <sub>CC</sub>	1.315	0.515	0.120×0.120
08	E	1.315	0.725	0.120×0.120
09	F	1.176	0.921	0.120×0.120
10	L	0.615	0.921	0.120×0.120
11	M	0.815	0.921	0.120×0.120
12	G	0.615	0.921	0.120×0.120
13	H	0.111	0.725	0.120×0.120
14	V <sub>DD</sub>	0.111	0.515	0.120×0.120

\* Note: Pad location is given as per passivation layer