



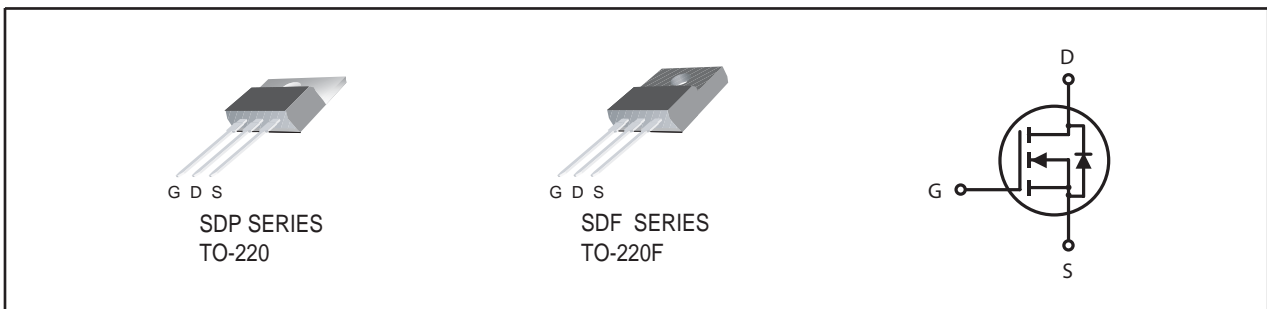
## N-Channel Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (Ω) Typ
600V	6A	1.3 @ V <sub>GS</sub> =10V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-220 and TO-220F Package.



### ORDERING INFORMATION

Ordering Code	Package	Marking Code	Delivery Mode	RoHS Status
SDP06N60HZ	TO-220	SDP06N60	Tube	Halogen Free
SDP06N60PZ	TO-220	06N60	Tube	Pb Free
SDF06N60HZ	TO-220F	SDF06N60	Tube	Halogen Free
SDF06N60PZ	TO-220F	06N60	Tube	Pb Free

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	SDP06N60	SDF06N60	Units
V <sub>DS</sub>	Drain-Source Voltage	600		V
V <sub>GS</sub>	Gate-Source Voltage	±30	±30	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	6	A
		T <sub>C</sub> =100°C	4.2	A
I <sub>DM</sub>	-Pulsed <sup>a</sup>	18	18	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>c</sup>	361		mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	107	W
		T <sub>C</sub> =100°C	54	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175		°C

### THERMAL CHARACTERISTICS

Symbol	Parameter	SDP06N60	SDF06N60	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.4	4.2	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

# SDP06N60

## SDF06N60

Ver 2.1

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =480V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±30V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =3A		1.3	1.6	ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =20V , I <sub>D</sub> =3A		5.2		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		855		pF
C <sub>oss</sub>	Output Capacitance			83		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			9		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =300V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		35		ns
t <sub>r</sub>	Rise Time			19		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			37		ns
t <sub>f</sub>	Fall Time			15		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		18		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		3.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			7.6		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =4A		0.82	1.4	V

### Notes

- Drain current limited by maximum junction temperature.
- Guaranteed by design, not subject to production testing.
- Starting T<sub>J</sub>=25°C, L=50mH, V<sub>DD</sub> = 50V. (See Figure 12)

Dec,24,2013

# SDP06N60

## SDF06N60

Ver 2.1

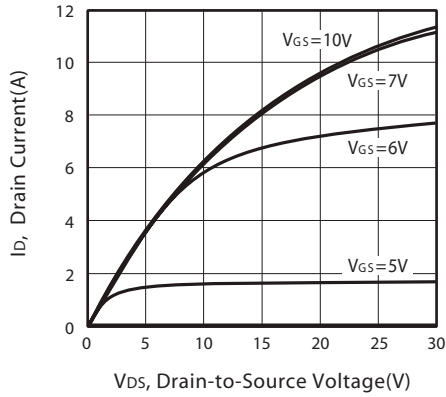


Figure 1. Output Characteristics

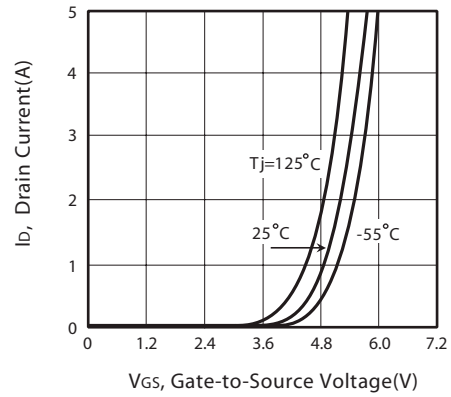


Figure 2. Transfer Characteristics

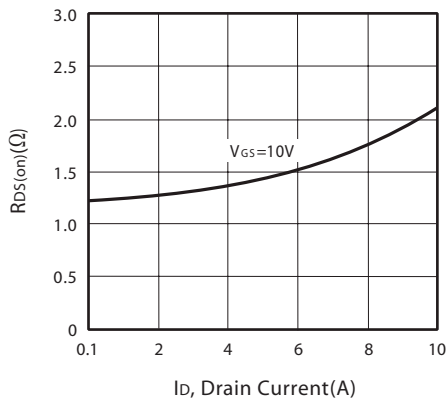


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

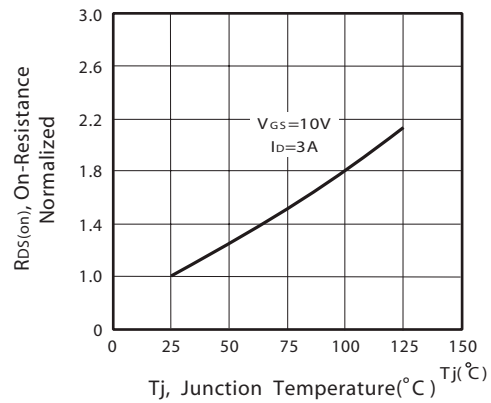


Figure 4. On-Resistance Variation with Drain Current and Temperature

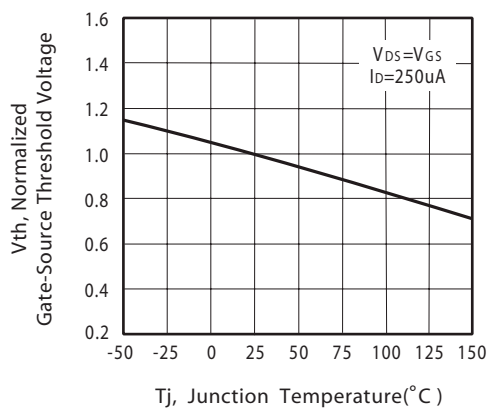


Figure 5. Gate Threshold Variation with Temperature

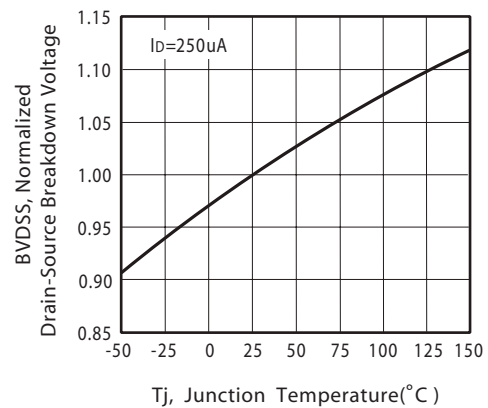


Figure 6. Breakdown Voltage Variation with Temperature

Dec,24,2013

# SDP06N60

## SDF06N60

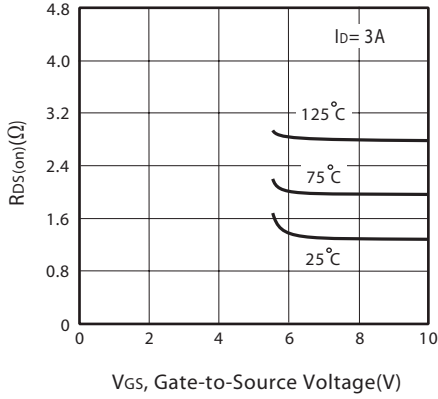


Figure 7. On-Resistance vs. Gate-Source Voltage

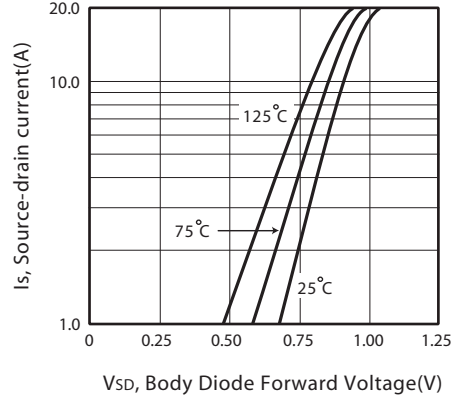


Figure 8. Body Diode Forward Voltage Variation with Source Current

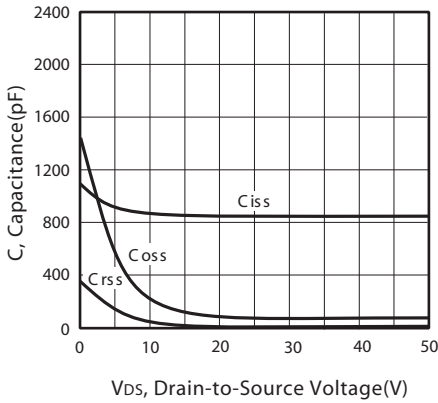


Figure 9. Capacitance

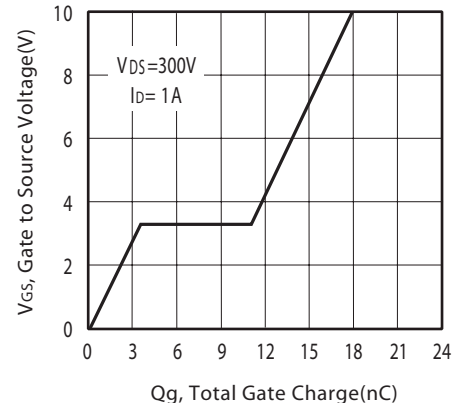


Figure 10. Gate Charge

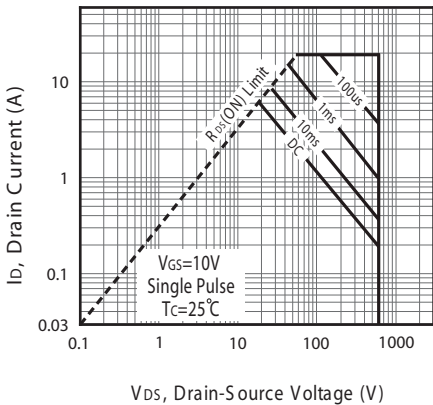


Figure 11a. Maximum Safe Operating Area for SDP06N60

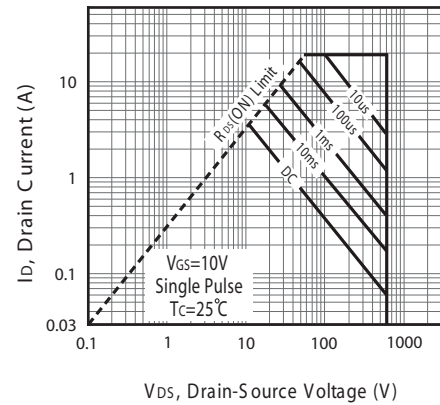
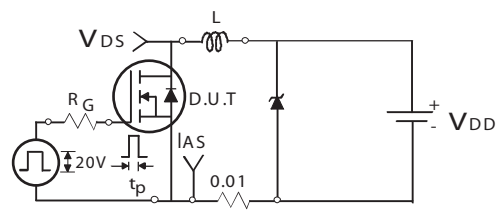


Figure 11b. Maximum Safe Operating Area for SDF06N60

# SDP06N60

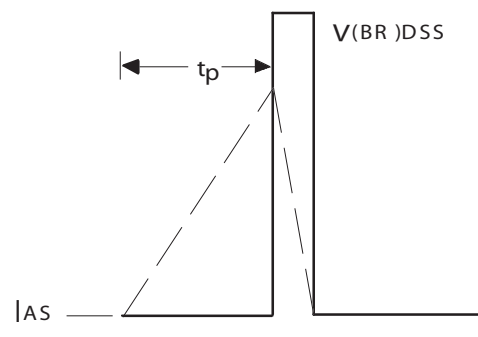
## SDF06N60

Ver 2.1



Unclamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

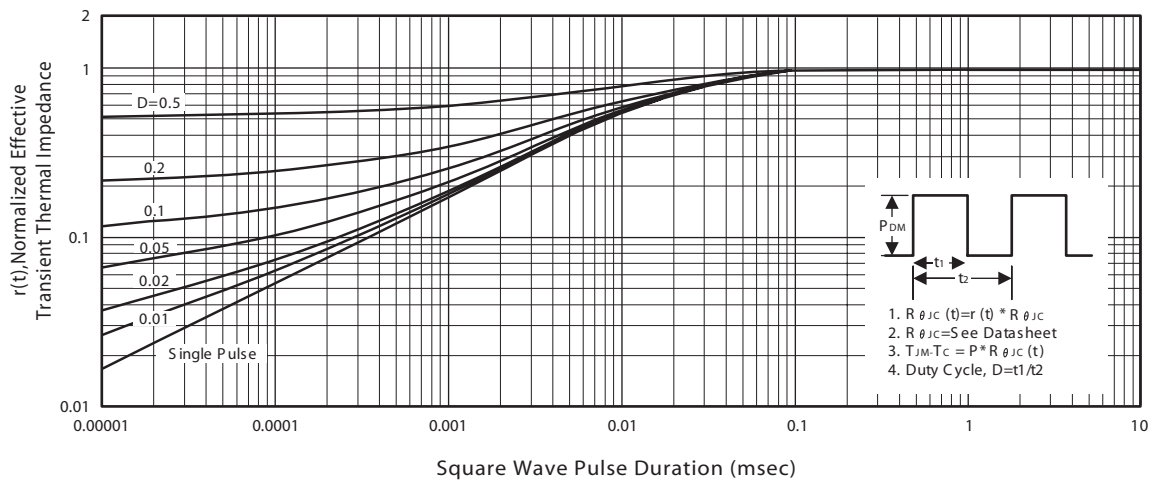


Figure 13a. Normalized Thermal Transient Impedance Curve for SDP06N60

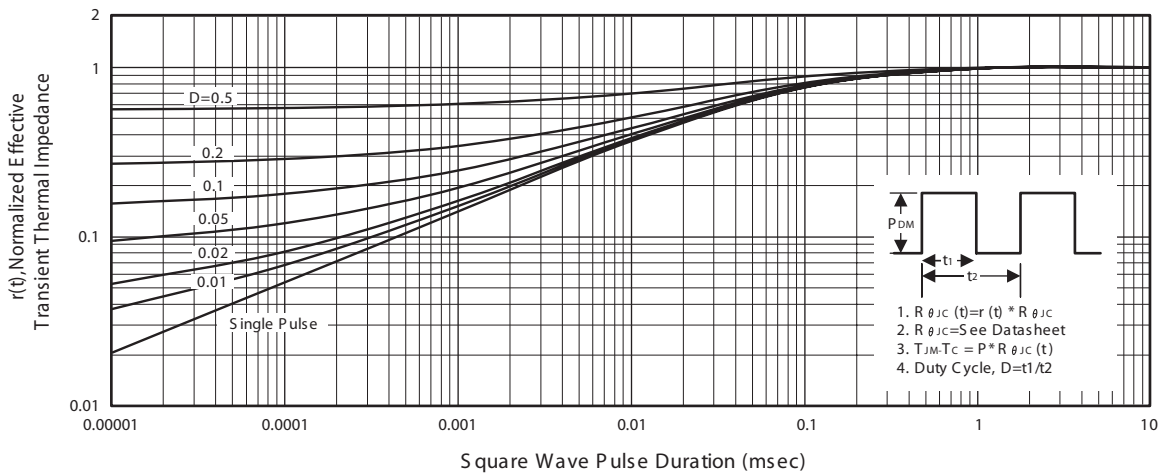


Figure 13b. Normalized Thermal Transient Impedance Curve for SDF06N60

Dec,24,2013

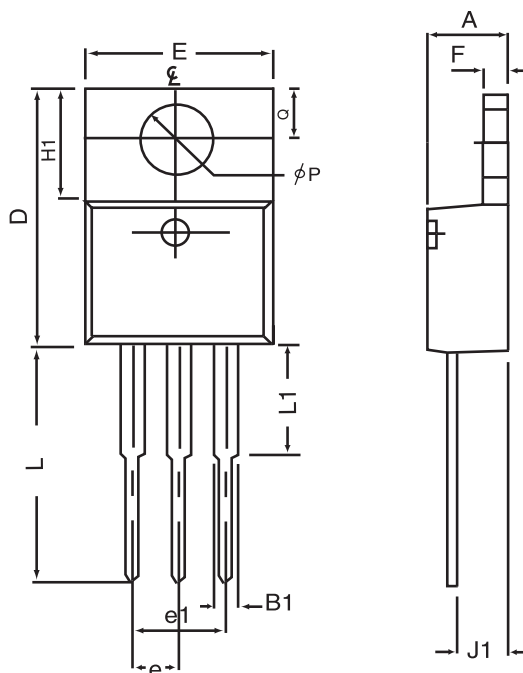
# SDP06N60

## SDF06N60

Ver 2.1

### PACKAGE OUTLINE DIMENSIONS

TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
$\phi P$	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

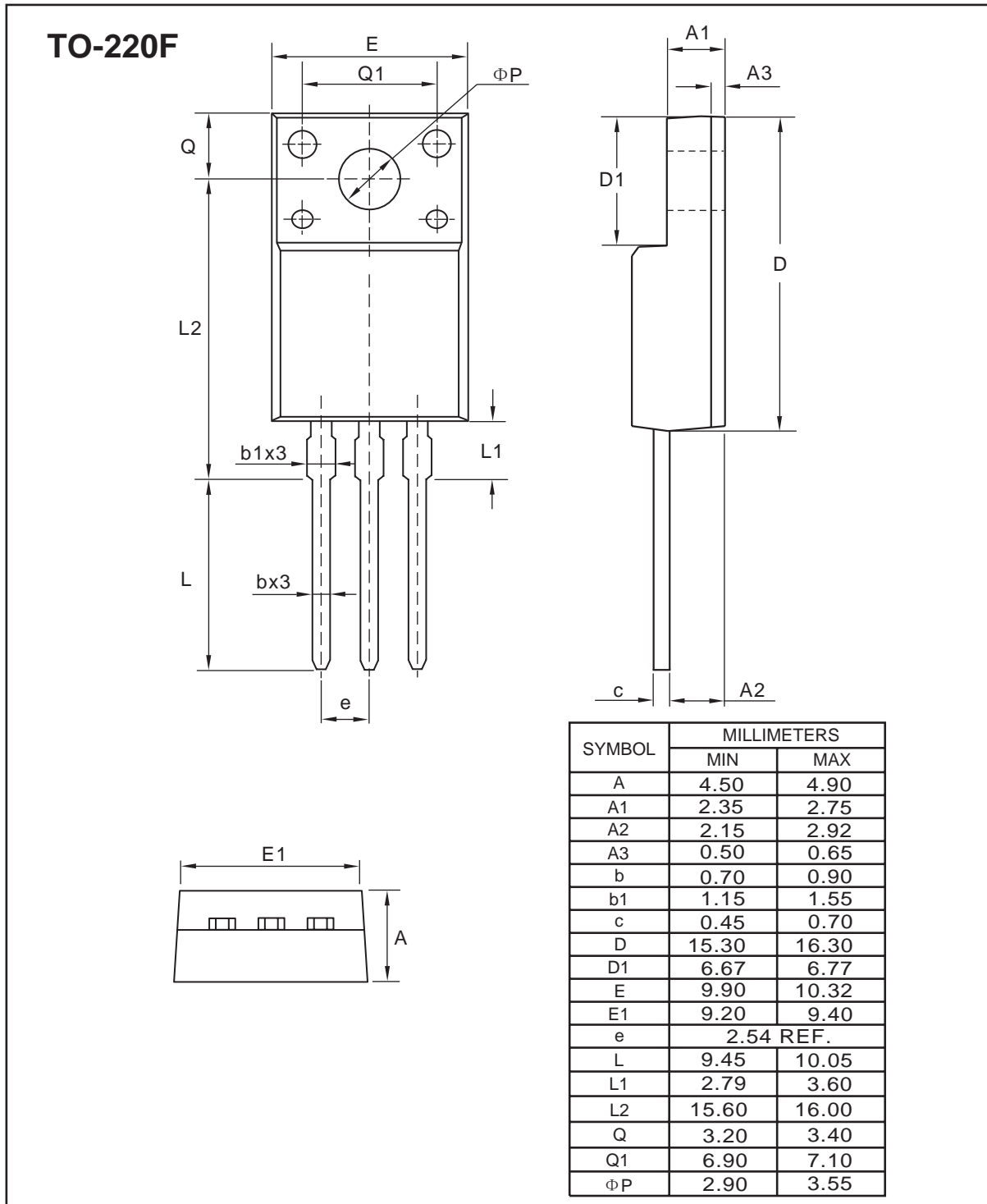
Dec,24,2013

# SDP06N60

## SDF06N60

Ver 2.1

### PACKAGE OUTLINE DIMENSIONS

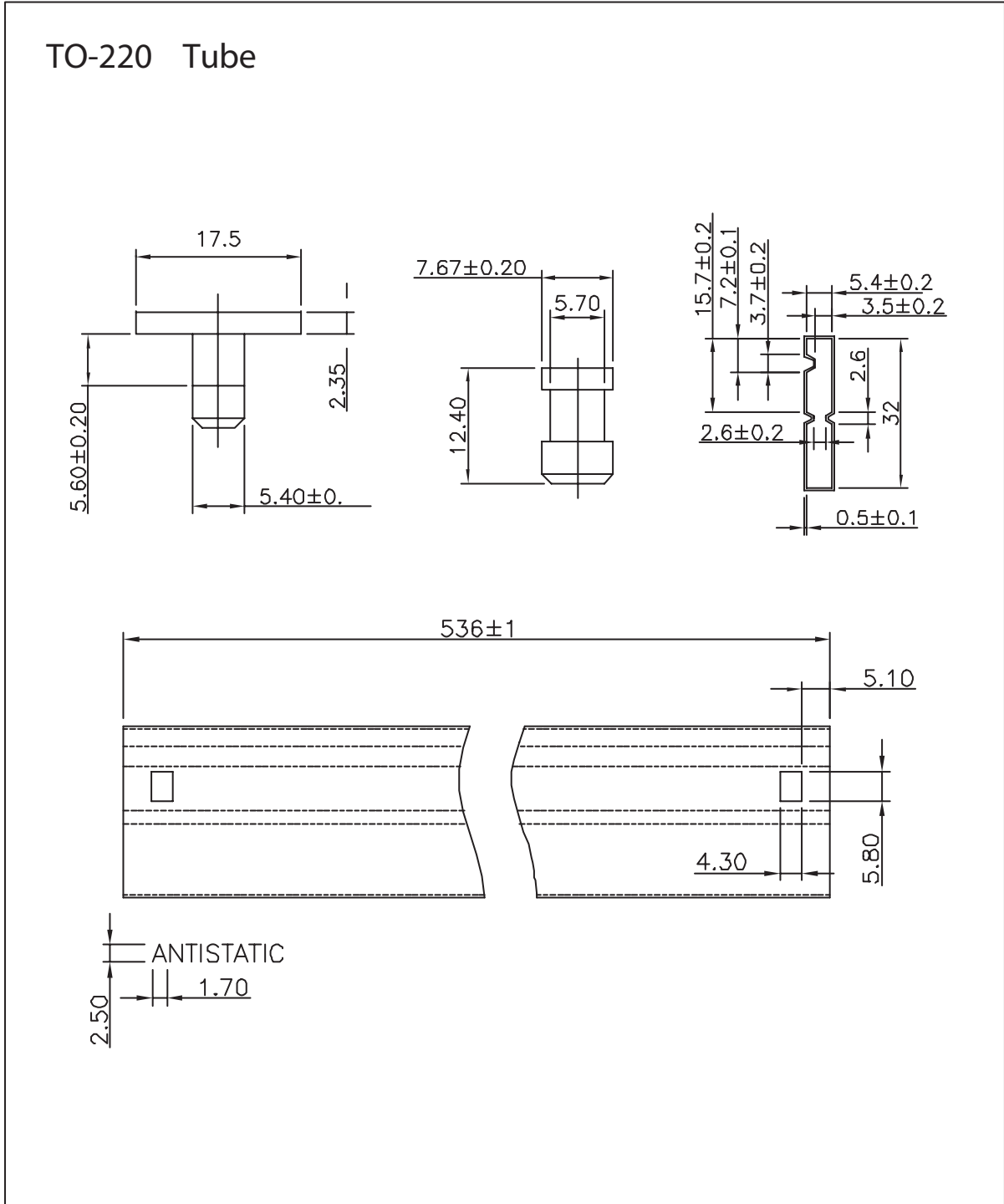


Dec,24,2013

# SDP06N60

## SDF06N60

Ver 2.1

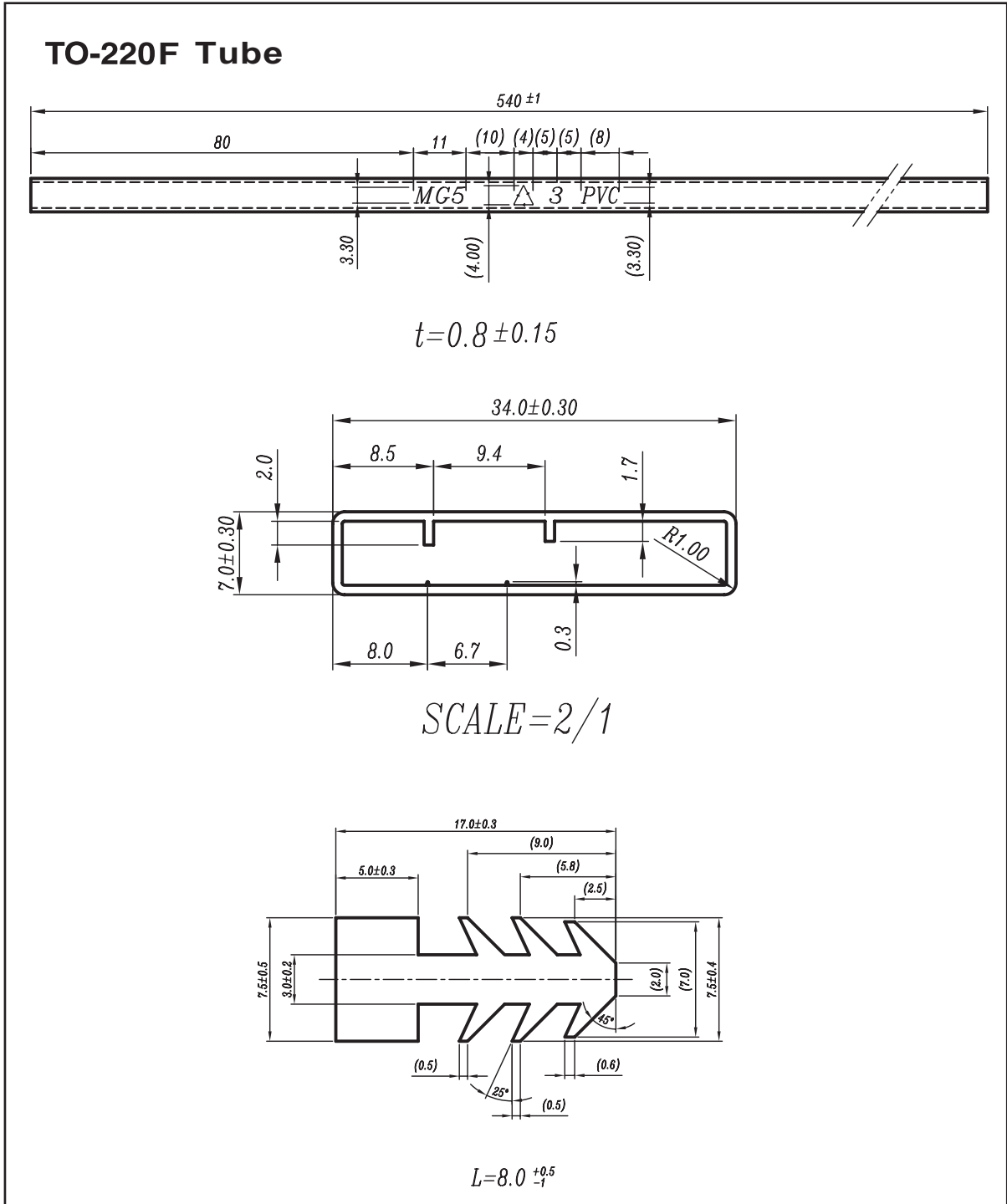


Dec,24,2013



**SDP06N60**  
**SDF06N60**

Ver 2.1



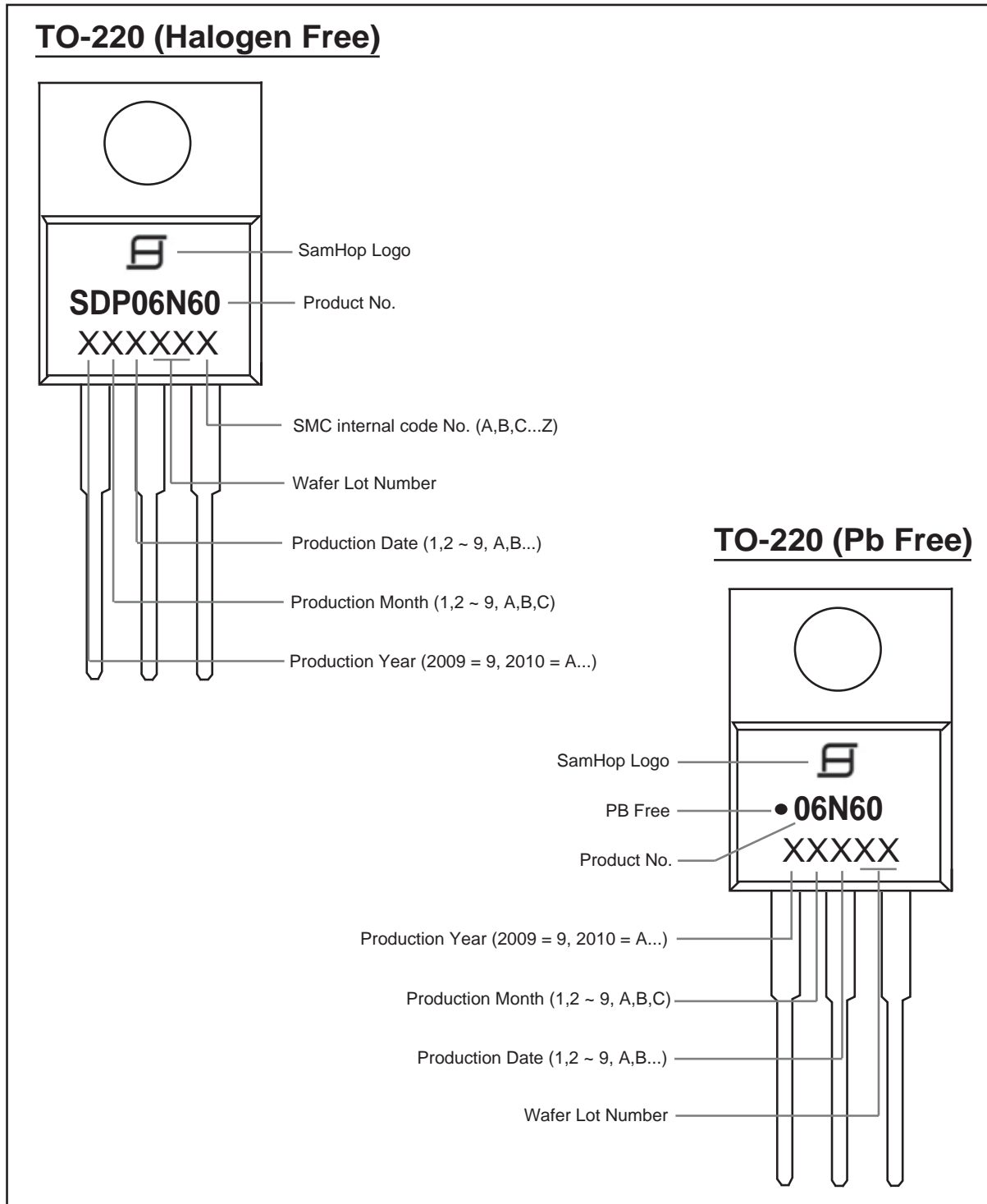
Dec,24,2013

# SDP06N60

# SDF06N60

Ver 2.1

## TOP MARKING DEFINITION



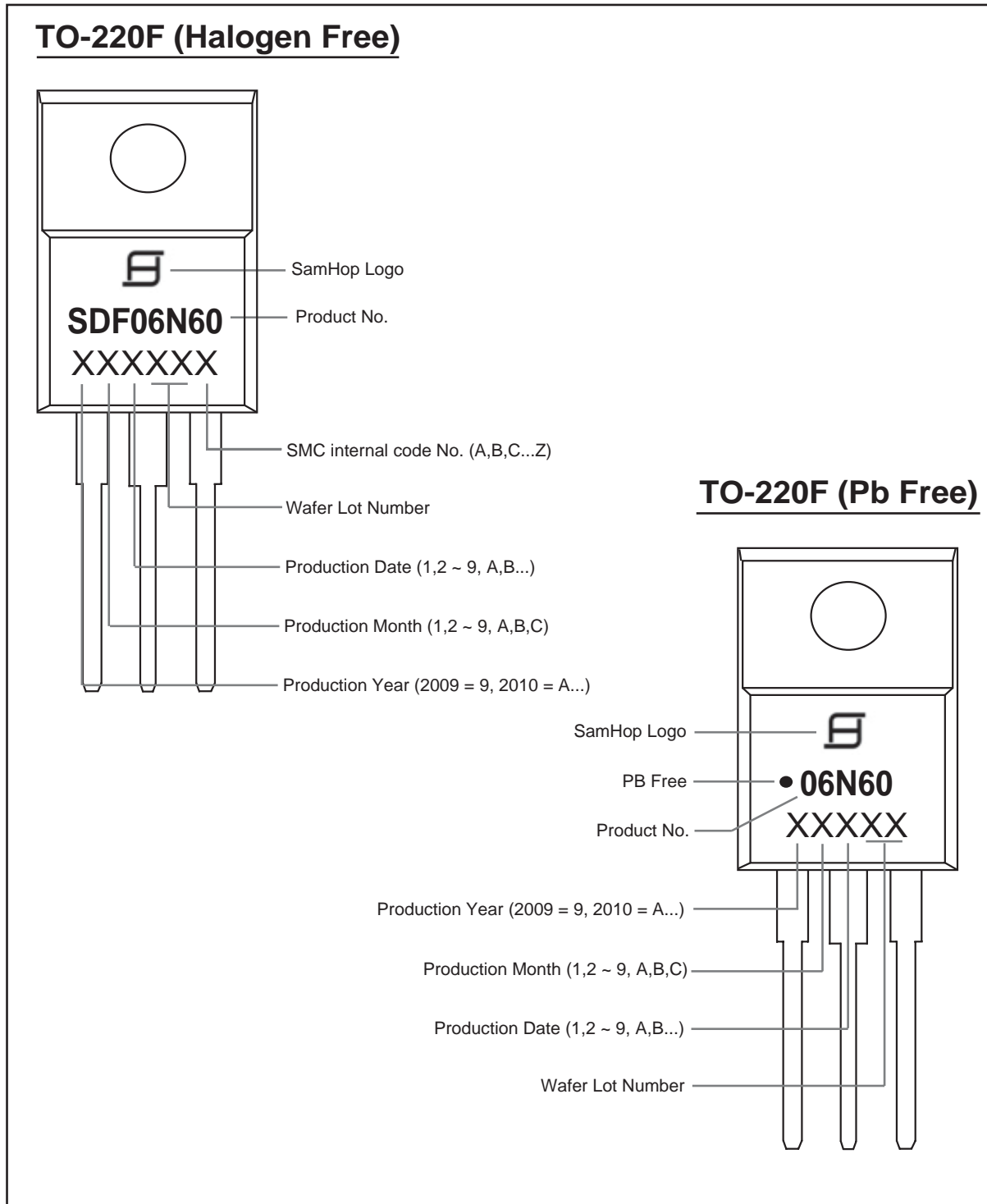
Dec,24,2013

# SDP06N60

# SDF06N60

Ver 2.1

## TOP MARKING DEFINITION



Dec,24,2013