

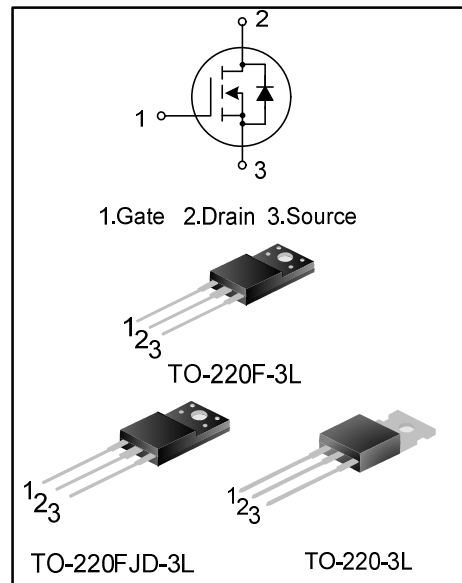
## 14A, 600V DP MOS POWER TRANSISTOR

### DESCRIPTION

SVSP14N60F(FJD)(T)D2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DPMOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

### FEATURES

- ◆ 14A,600V,  $R_{DS(on)(typ.)}=0.25\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVSP14N60TD2	TO-220-3L	P14N60TD2	Halogen free	Tube
SVSP14N60FJDD2	TO-220FJD-3L	P14N60FJD	Halogen free	Tube
SVSP14N60FD2	TO-220F-3L	P14N60FD2	Halogen free	Tube

### ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^\circ\text{C}$ )

Characteristics	Symbol	Ratings		Unit
		SVSP14N60TD2	SVSP14N60F/FJDD2	
Drain-Source Voltage	$V_{DS}$	600		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	14	A
		$T_C=100^\circ\text{C}$	8.8	
Drain Current Pulsed	$I_{DM}$	56		A
Power Dissipation ( $T_C=25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	$P_D$	120	38	W
		0.96	0.3	
Single Pulsed Avalanche Energy (Note1)	$E_{AS}$	580		mJ
Reverse diode dv/dt (Note 2)	dv/dt	15		V/ns
MOSFET dv/dt ruggedness(Note 3)	dv/dt	50		V/ns
Operation Junction Temperature Range	$T_J$	-55~+150		$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55~+150		$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Value		Unit
		SVSP14N60TD2	SVSP14N60F/FJDD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.04	3.29	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C/W

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^\circ\text{C}$ )

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=600V, V_{GS}=0V$	--	--	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=7.0A$	--	0.25	0.28	$\Omega$
		$T_j=125^\circ\text{C}$	--	0.51	--	
Input Capacitance	$C_{iss}$	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=100V$	--	805	--	pF
Output Capacitance	$C_{oss}$		--	48	--	
Reverse Transfer Capacitance	$C_{rss}$		--	3.2	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V, V_{GS}=10V, R_G=24\Omega, I_D=14A$ (Note 4,5)	--	14	--	ns
Turn-on Rise Time	$t_r$		--	52	--	
Turn-off Delay Time	$t_{d(off)}$		--	117	--	
Turn-off Fall Time	$t_f$		--	43	--	
Total Gate Charge	$Q_g$	$V_{DD}=480V, V_{GS}=10V, I_D=14A$ (Note 4,5)	--	26	--	nC
Gate-Source Charge	$Q_{gs}$		--	6.0	--	
Gate-Drain Charge	$Q_{gd}$		--	13	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	11	A
Pulsed Source Current	$I_{SM}$		--	--	56	
Diode Forward Voltage	$V_{SD}$	$I_S=14A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$V_{DD}=50V, I_F=14A, dl_f/dt=100A/\mu s$	--	378	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	4.6	--	$\mu C$

### Notes:

- $L=79\text{mH}, I_{AS}=3.5A, V_{DD}=100V, R_G=25\Omega$ , starting temperature  $T_j=25^\circ\text{C}$ ;
- $V_{DS}=0\sim 400V, I_{SD}\leq 14A, T_j=25^\circ\text{C}$ ;
- $V_{DS}=0\sim 480V$ ;
- Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycles  $\leq 2\%$ ;
- Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

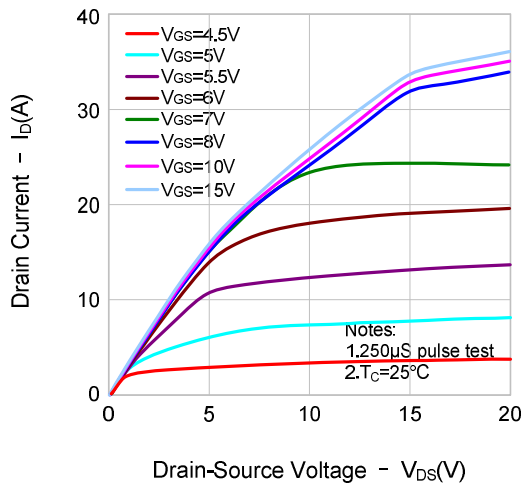


Figure 2. Transfer Characteristics

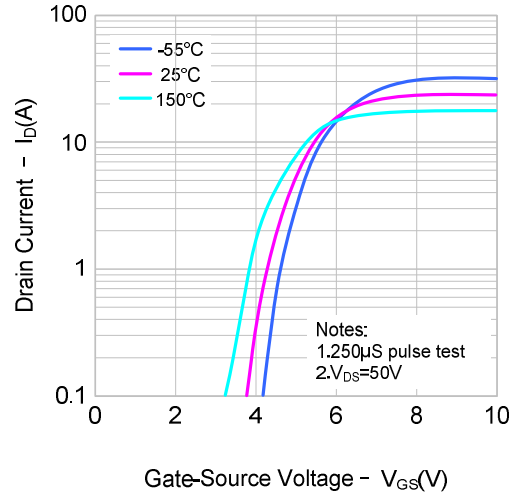


Figure 3. On-Resistance Variation vs. Drain Current

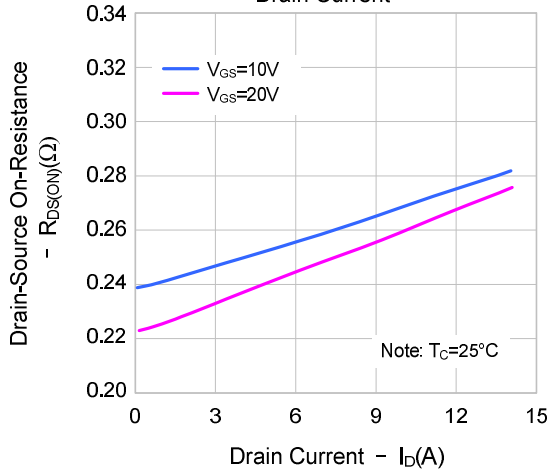


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

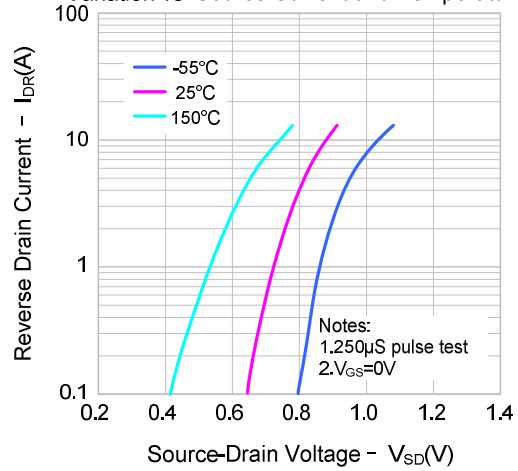


Figure 5. Capacitance Characteristics

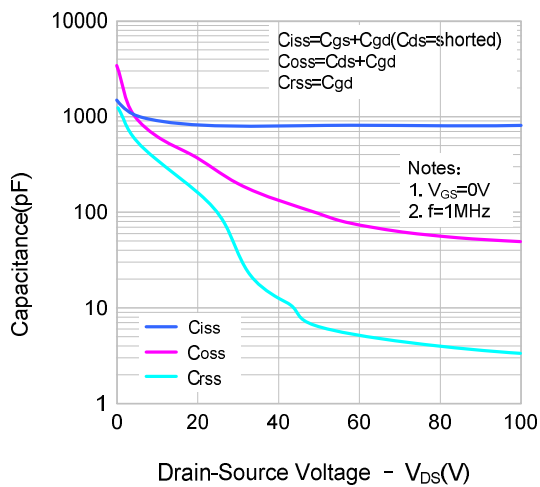
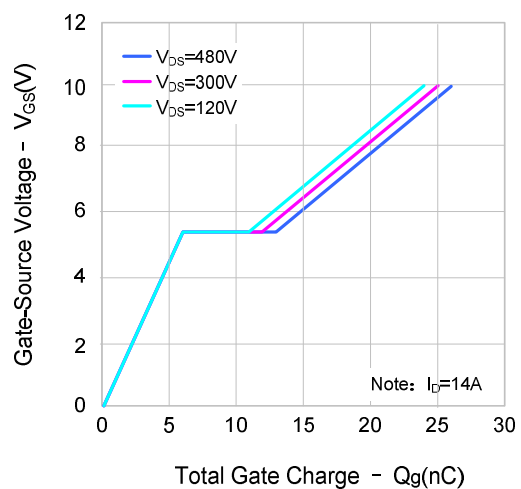


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

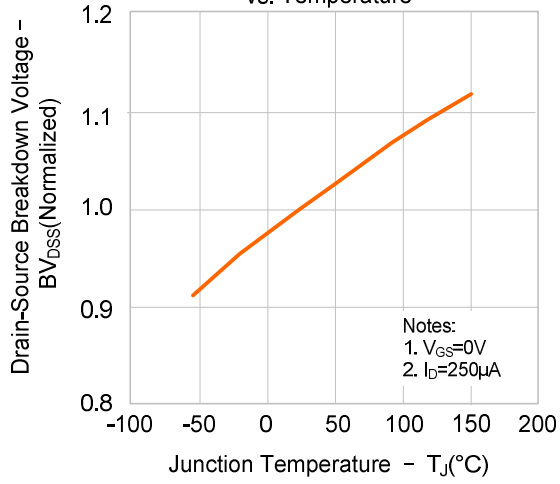


Figure 8. On-resistance Variation vs. Temperature

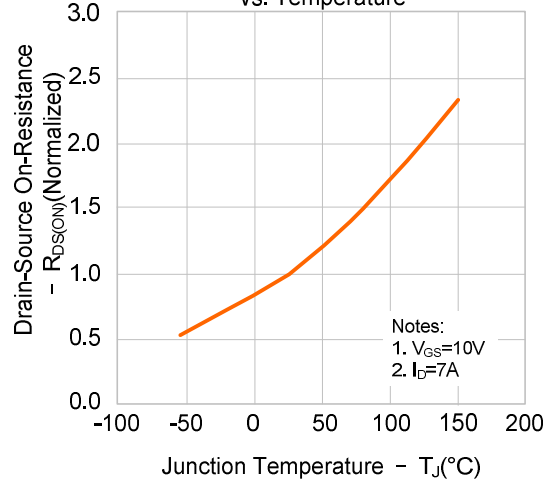


Figure 9-1. Max. Safe Operating Area(SVSP14N60TD2)

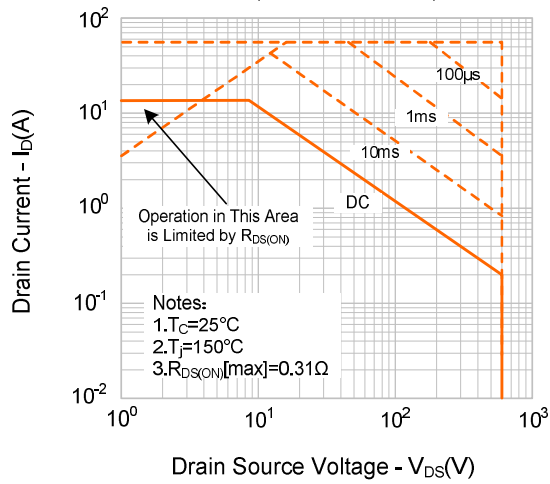
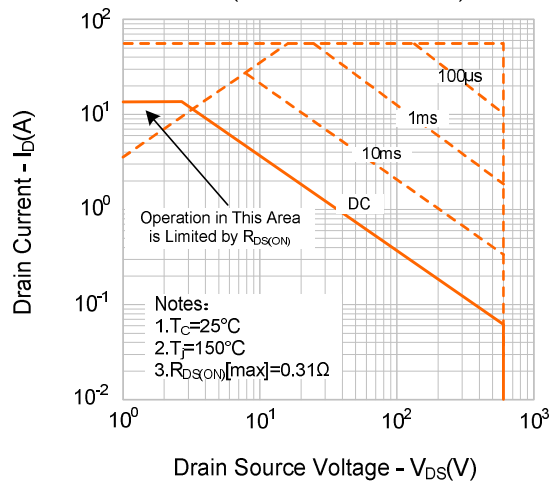
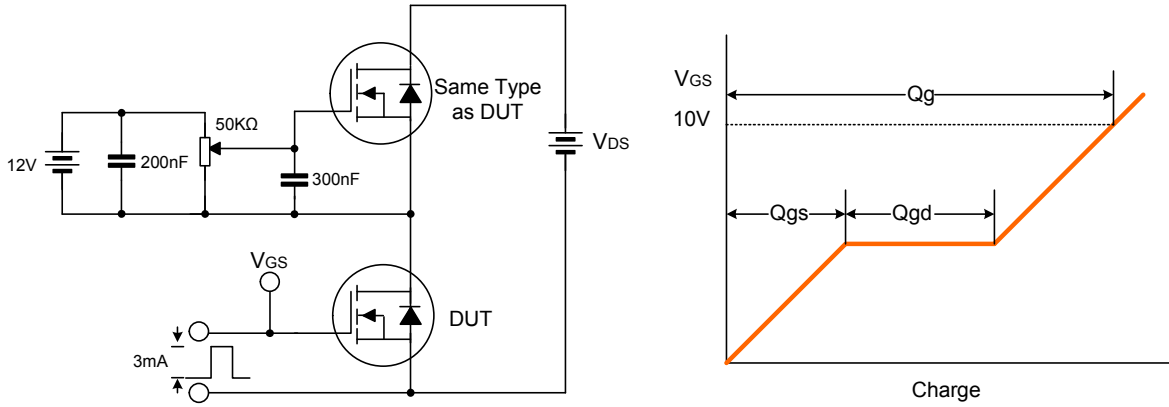


Figure 9-2. Max. Safe Operating Area(SVSP14N60F/FJDD2)

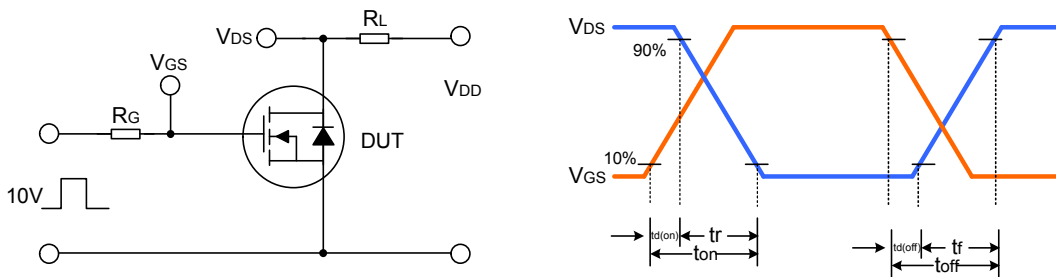


**TYPICAL TEST CIRCUIT**

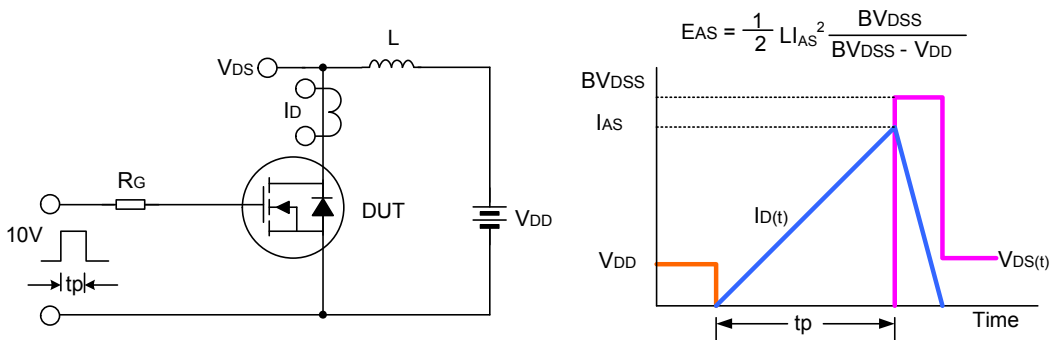
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



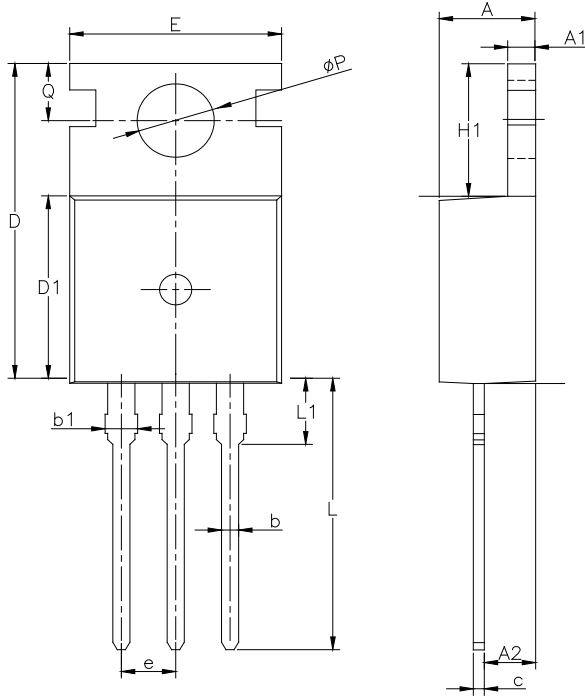
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

**TO-220-3L**

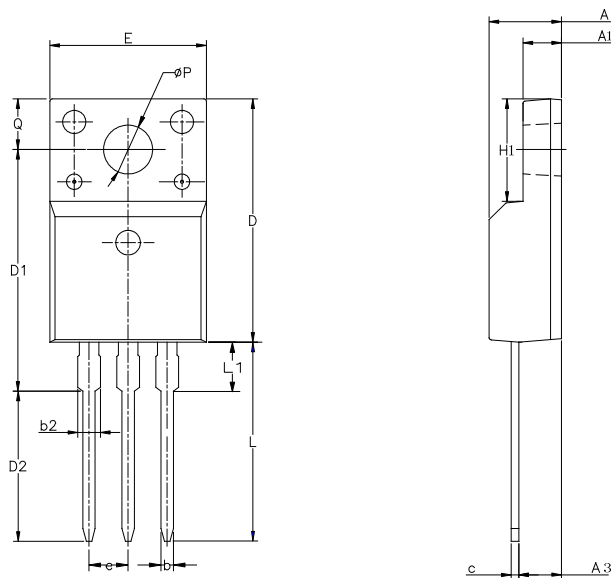
**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
$\phi P$	3.40	3.70	3.90
Q	2.60	—	3.20

**TO-220FJD-3L**

**UNIT: mm**

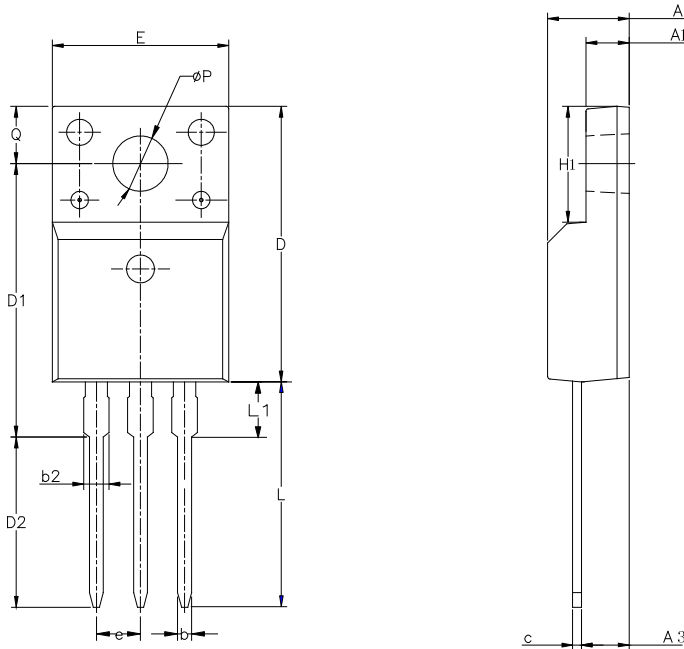


SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

**PACKAGE OUTLINE(continued)**

**TO-220F-3L**

**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

**Disclaimer :**

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Rev.: 1.0

Revision History:

1. First release
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