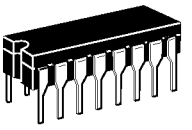
MC14538B

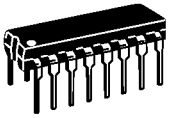
Dual Precision Retriggerable/Resettable Monostable Multivibrator

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

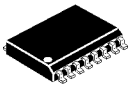
- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative–Going Edge (B–Input)
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10 μs with Supplies Up to 6 V.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
*MC14XXXBDW	SOIC

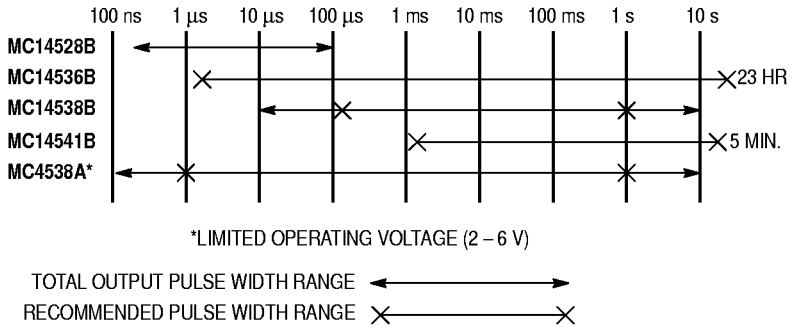
T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

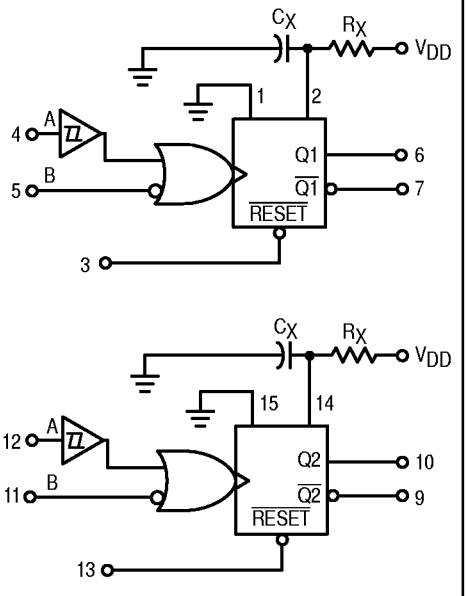
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

ONE–SHOT SELECTION GUIDE



BLOCK DIAGRAM



R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

* Consult factory for possible "D" suffix SOIC Case 751B.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current, Pin 2 or 14	I_{in}	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	µAdc
Input Current, Other Inputs	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance, Pin 2 or 14	C_{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Q = Low, $\overline{Q}$ = High	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current, Active State (Both) (Per Package) Q = High, $\overline{Q}$ = Low	I_{DD}	5.0	—	2.0	—	0.04	0.20	—	2.0	mAdc
		10	—	2.0	—	0.08	0.45	—	2.0	
		15	—	2.0	—	0.13	0.70	—	2.0	
**Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X)	I_T	5.0	$I_T = (3.5 \times 10^{-2})\ R_X C_X f + 4 C_X f + 1 \times 10^{-5}\ C_L f$							µAdc
		10	$I_T = (8.0 \times 10^{-2})\ R_X C_X f + 9 C_X f + 2 \times 10^{-5}\ C_L f$							
			$I_T = (1.25 \times 10^{-1})\ R_X C_X f + 12 C_X f + 3 \times 10^{-5}\ C_L f$							
			where: I_T in µA (one monostable switching only), C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
**The formulas given are for the typical characteristics only at 25°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
A or B to Q or $\overline{Q}$	t_{PHL}					
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	220	
$\overline{Reset}$ to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0	—	250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	—	95	190	
Input Rise and Fall Times	t_r, t_f	5	—	—	15	µs
$\overline{Reset}$		10	—	—	5	
		15	—	—	4	
B Input		5	—	300	1.0	ms
		10	—	1.2	0.1	
		15	—	0.4	0.05	
A Input		5	No Limit			—
		10				
		15				
Input Pulse Width	t_{WH},	5.0	170	85	—	ns
A, B, or Reset	t_{WL}	10	90	45	—	
		15	80	40	—	
Retrigger Time	t_{rr}	5.0	0	—	—	ns
		10	0	—	—	
		15	0	—	—	
Output Pulse Width — Q or $\overline{Q}$	T					µs
Refer to Figures 8 and 9						
C_X = 0.002 µF, R_X = 100 kΩ		5.0	198	210	230	
		10	200	212	232	
		15	202	214	234	
C_X = 0.1 µF, R_X = 100 kΩ		5.0	9.3	9.86	10.5	ms
		10	9.4	10	10.6	
		15	9.5	10.14	10.7	
C_X = 10 µF, R_X = 100 kΩ		5.0	0.91	0.965	1.03	s
		10	0.92	0.98	1.04	
		15	0.93	0.99	1.06	
Pulse Width Match between circuits in	100	5.0	—	± 1.0	± 5.0	%
the same package.	$[(T_1 - T_2)/T_1]$	10	—	± 1.0	± 5.0	
C_X = 0.1 µF, R_X = 100 kΩ		15	—	± 1.0	± 5.0	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	—	5.0	—		kΩ
External Timing Capacitance	C_X	—	0	—	No Limit†	µF

* The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for R_X > 1 MΩ..
†If C_X > 15 µF, use discharge protection diode per Fig. 11.

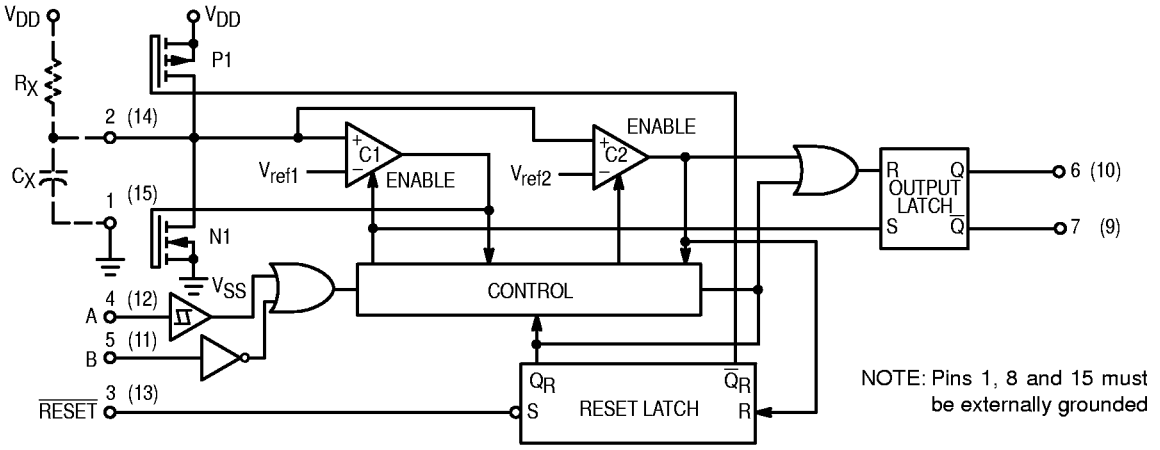


Figure 1. Logic Diagram (1/2 of Device Shown)

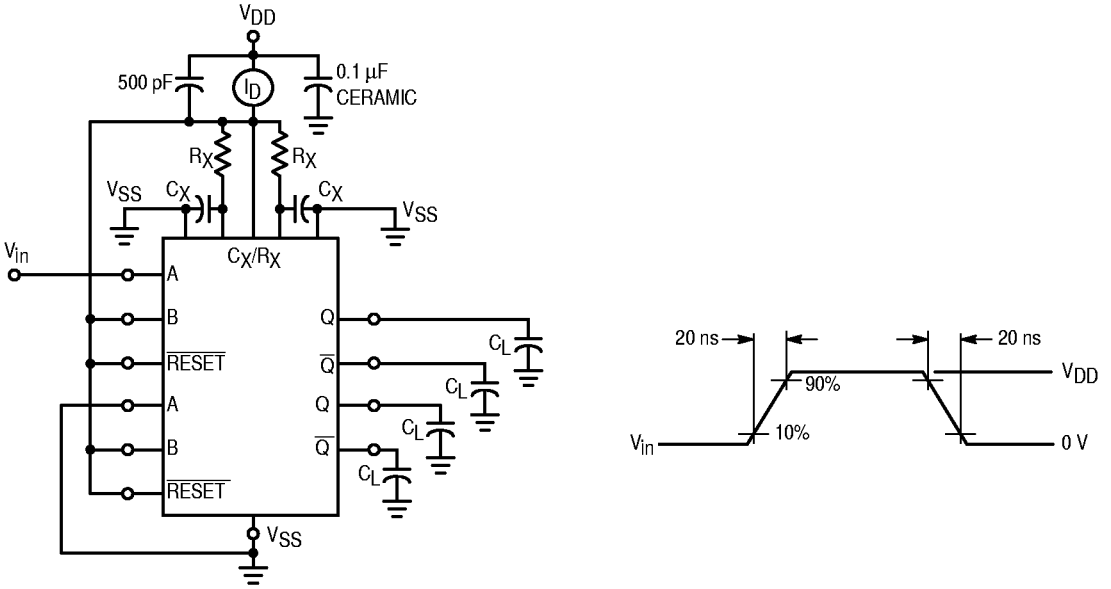
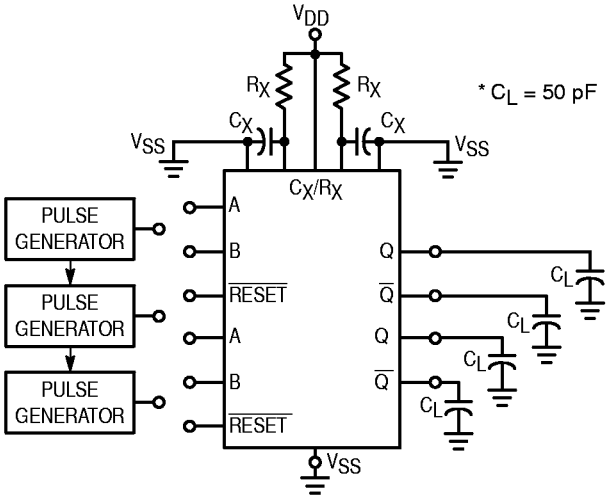


Figure 2. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

* Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown In Figure 4.

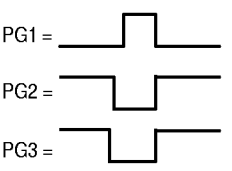


Figure 3. Switching Test Circuit

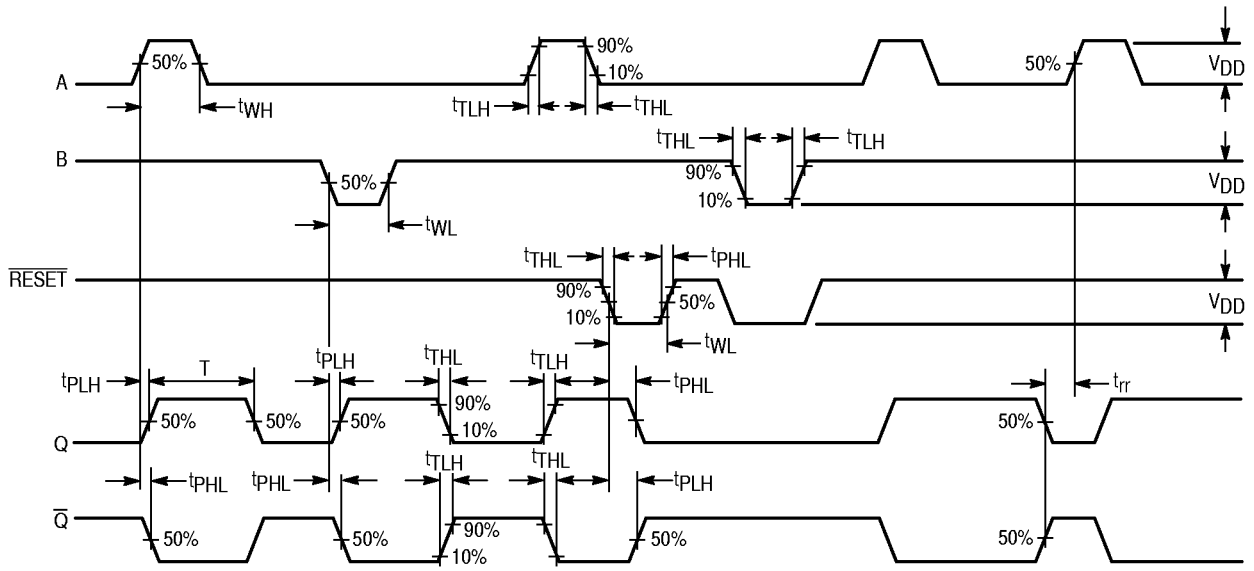


Figure 4. Switching Test Waveforms

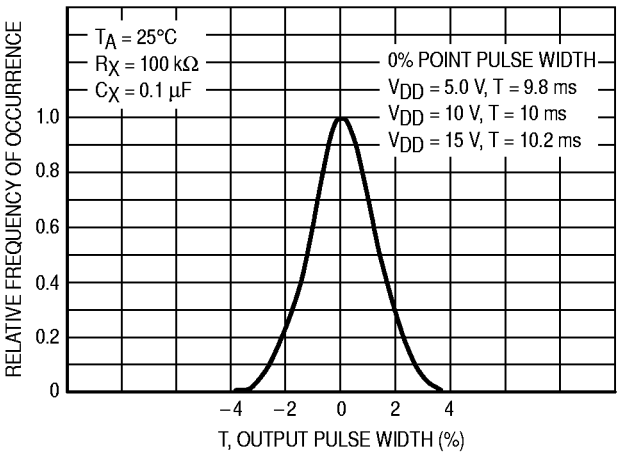


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

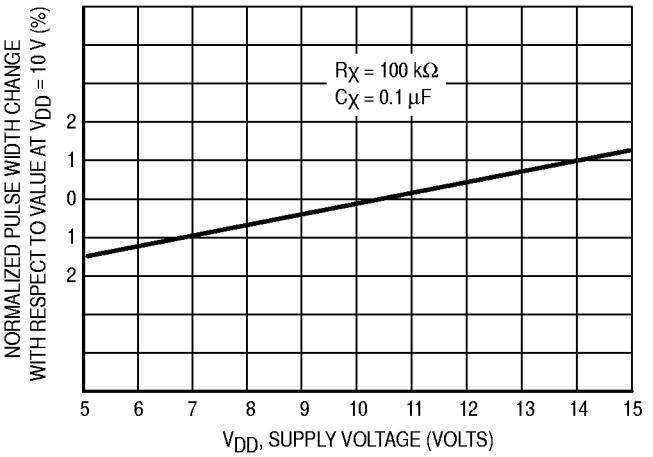


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

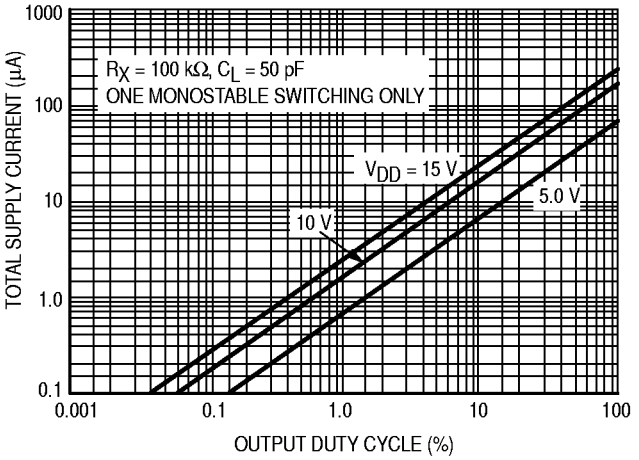


Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{Q}$
H	↗	H	⊓	⊔
H	L	↘	⊓	⊔
H	↗↘	L	Not Triggered	
H	H	↗↘	Not Triggered	
H	L, H, ↘	H	Not Triggered	
H	L	L, H, ↗	Not Triggered	
L	X	X	L	H
↘↗	X	X	Not Triggered	

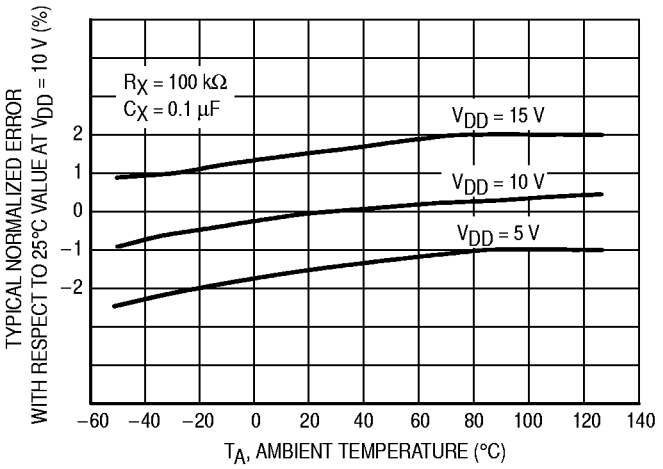


Figure 8. Typical Error of Pulse Width Equation versus Temperature

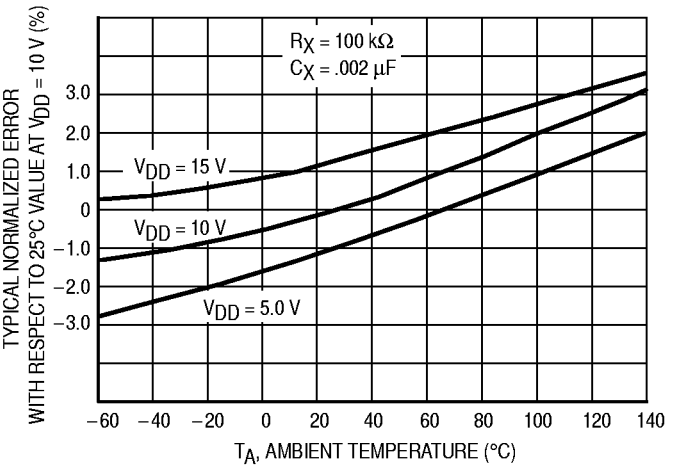


Figure 9. Typical Error of Pulse Width Equation versus Temperature

THEORY OF OPERATION

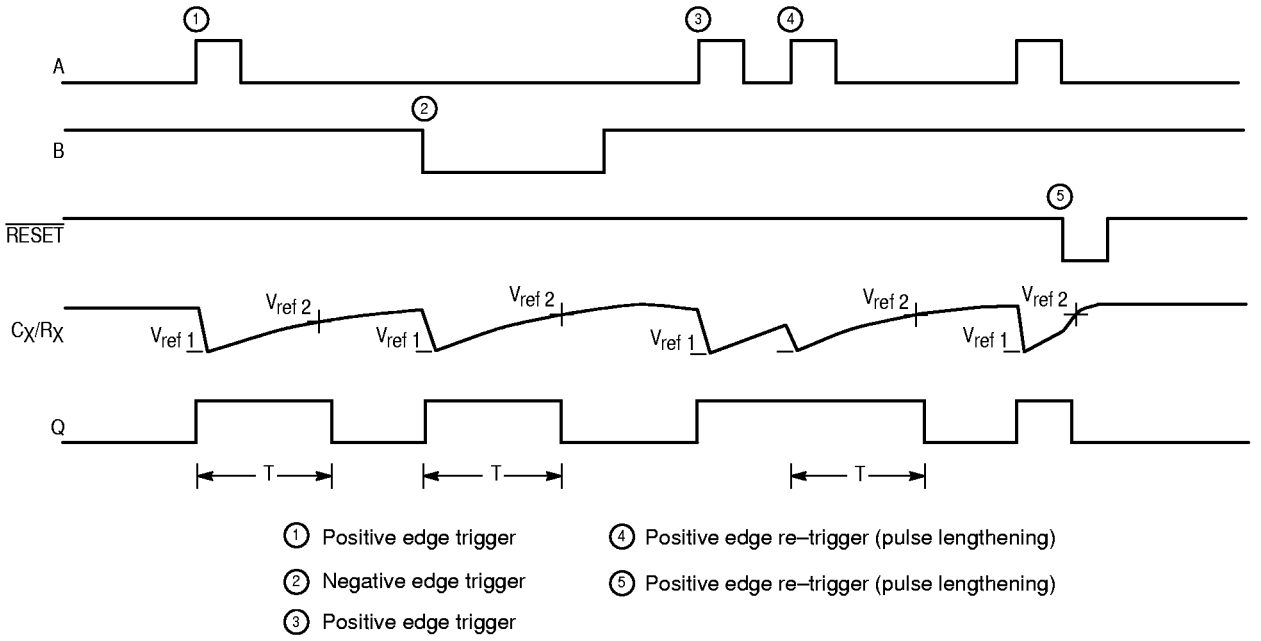


Figure 10. Timing Operation

TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{\text{Reset}}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N–channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\,2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at C_X/R_X will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{\text{Reset}}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the reset latch will clear, and will then be ready to accept another pulse. It the $\overline{\text{Reset}}$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{\text{Reset}}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER–DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than (V_{DD}). (C)/(10 mA). For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) x (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X, connected as shown in Fig. 11.

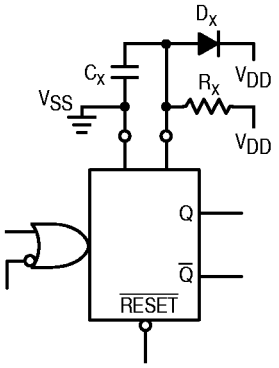
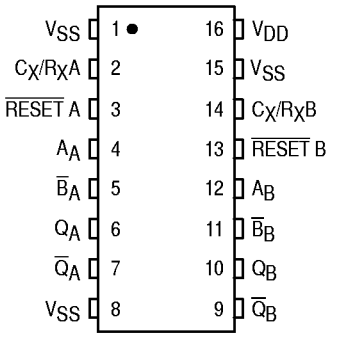


Figure 11. Use of a Diode to Limit Power Down Current Surge

PIN ASSIGNMENT



TYPICAL APPLICATIONS

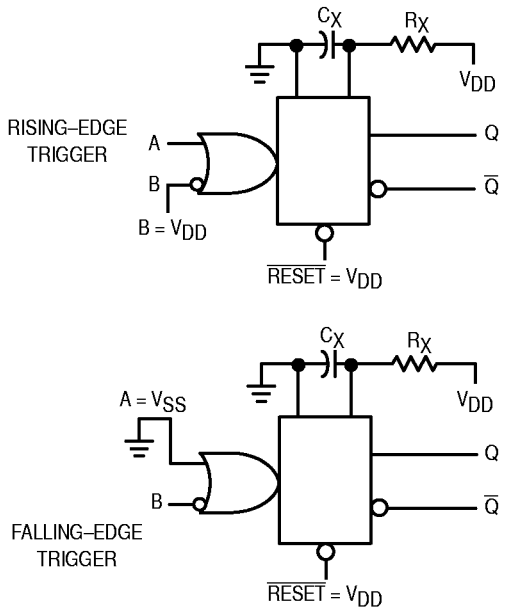


Figure 12. Retriggerable Monostables Circuitry

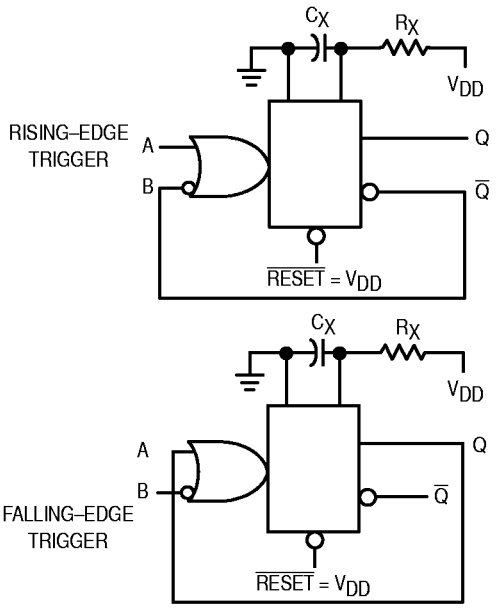


Figure 13. Non–Retriggerable Monostables Circuitry

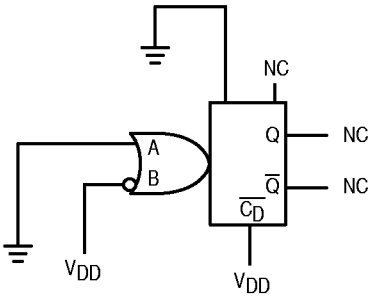
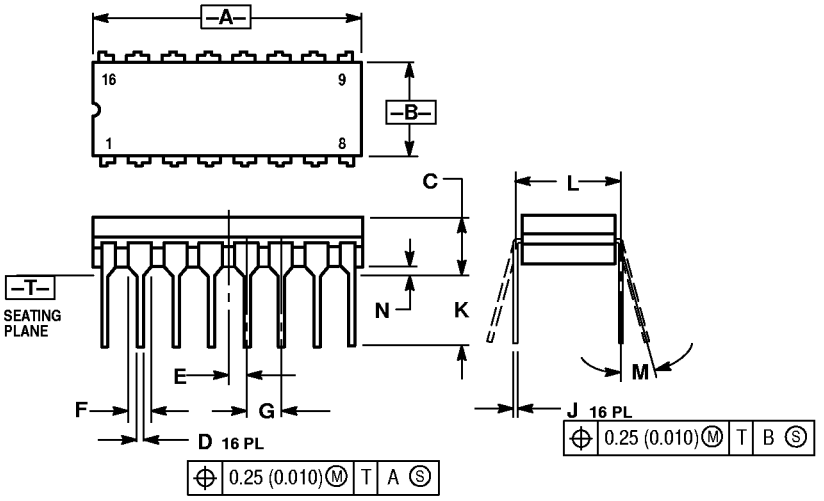


Figure 14. Connection of Unused Sections

OUTLINE DIMENSIONS

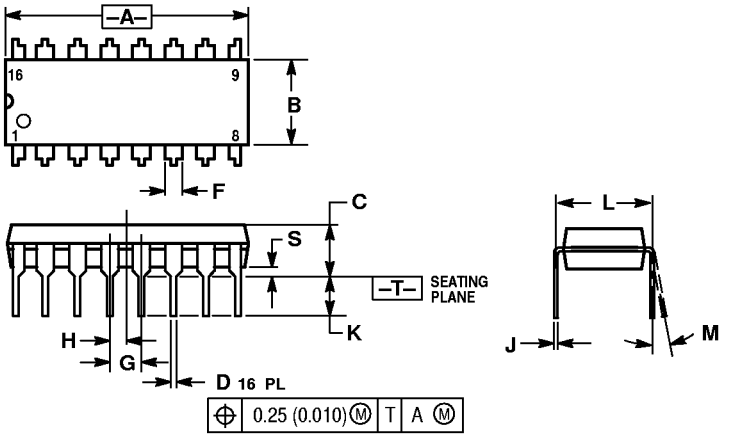
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

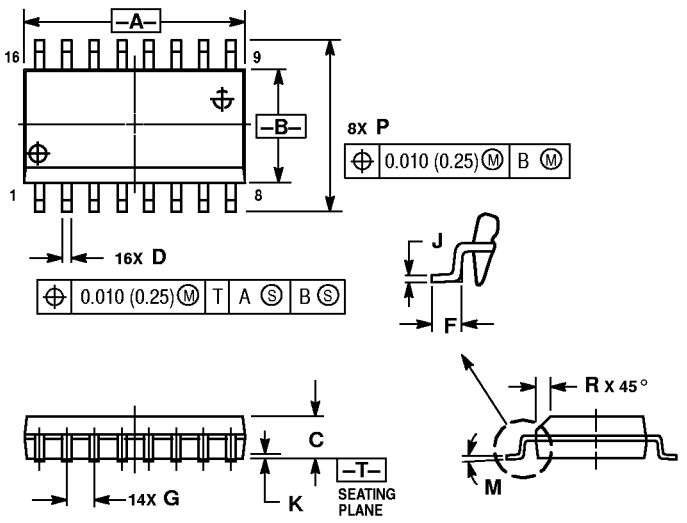


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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